MARKET NOTES

William Bricken
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Bullets for presentation are in first section, the rest is bulk data.

CONTENTS

Sources

- a dozen text books
- corporate SEC reports
- accumulated product information and whitepapers
- several academic courses

WHY BUY BTC INSTEAD OF CPLD

The complete range of potential BTC products could challenge the entire semiconductor marketplace. We elect to enter the semiconductor market with generic reconfigurable logic chips that accommodate up to 100K gates and are not mass commodity items.

Here are some reasons for this strategic decision.

MARKETABLE

fastest product time-to-market
most developed product currently (i.e. hardware simulation)
highest potential profit margin
lowest risk
lowest cost of development
strong advantage in solving the SPLD scaling problem
clear product differentiation (not an FPGA, not a CPLD)

TECHNICAL

free design software
known propagation delay
low price
dynamic reprogramability and reconfiguration

solves major problems of other architectures
SPLD: does not scale, fixed architecture
CPLD: limited registers, poor interconnect mapping and timing
FPGA: unpredictable interconnect mapping and timing
ASIC: high NRE and long development time
uP: extreme inefficiency, no parallelism

STORY

All the CPLD/FPGA architectures are trying to accommodate for logic expressability because they don't have appropriate minimization and transformation tools. Thus they create confusing and complex logic structures.

INTERESTING DATA

2000 world-wide digital IC market = $174B
    world-wide logic = $44B
        standard logic
        custom ASICs (gate-arrays, standard cells, full custom)
        PLD

PLD market in 2000 = $4.1B (Dataquest)
    low-density SPLDs = $0.2B low = <1K gates
    high-density CPLDs = $1.2B
    high-density FPGAs = $2.7B

Makimoto (Sony):
    IC market swings between standardization and customization
        57-67 standard discretes
        67-77 custom LSIs (TVs, calculators)
        77-87 standard microprocessors, memories
        87-97 custom ASICs
        97-07 field programmability
            standardized manufacturing
            customized to application

Essential economic issue:
    must waste transistors cause decreasing die size will
        decrease revenues for entire industry
    constant die size = constant biz economic
    shrinking die size = shrinking revenue for both vendors and resellers

Product differentiation is achieved only in logic. uP and memory architectures are basically the same.

Quicksilver: Altera and Xilinx have ignored dynamic logic market cause
    can't meet demand for regular products
    focus on high margin high-end
    no incentive to design dynamic logic cause no demand

Cost of fabbed wafer:
    $.4B per acre, sells for $1B per acre
    1 nano-acre = 4 mm^2

Over 300 unique CPLD and FPGA architectures

98% of the uP market is in embedded systems

FlashROM uses more power than SRAM

PLDs are standard products, off-the-shelf. Provides product differentiation without sacrificing time-to-market.

I-CUBE
- has low-power high-performance crosspoint switch
- exactly like CCA

Some vendor proprietary features
- CPLD
  - robust switching matrix
  - wide signal fanin
  - macrocell register configurability
  - supplemental product terms
- FPGA
  - fast multipliers
  - carry chains
  - delay-lock loops
  - PLLs

FIFOs dominate chip area
- i/o buffering is much bigger than logic
- FIFOs dominate floor-planning and dataflow and pin-locations

CHARACTERIZATION OF VARIOUS COMPETITORS

XILINX
- net revenues up 62% due to SpartanII and Virtex
- advanced products = 34% of revenues (.25um and smaller)
- advanced products = $846M
- gross margin = 51%
- position increasingly dependent on global economy
- fabless
- targeting ASICs with low-cost FPGAs (i.e. Spartan)
- ease of design is a major competitive advantage [!]
- license out older technologies
- litigation:
  - Altera (won)
  - Altera is suing them (c 2000)
  - employees who went to Altera

ALTERA
- Apex family is CPLD/FPGA hybrid
- gross margin 66%
- customers prefer low voltage
- new products = 4% of sales
- mainstream products up 285%, while price decrease of 33%
- strong sales in networking and telecommunications
- teamed with Cypress

low yields for new products, trouble with fab
bought share of fab house
customers increasingly use standard cell ASICs for integration
impeding their penetration and displacing their products
litigation with Xilinx (lost and resued) over new products FLEX
AMD and Lattice team
sued Clearlogic

LATTICE
76% 2000 revenues from CPLDs
after wafer fab
they ship them to independent (Asia) contractors for assembly
and then to different contractors for testing
competitive factors
product features
density
speed
power consumption
reprogramability
design flexibility
design reliability
price
market acceptance
customer support
sales, marketing and distribution strength
On their board:
Larry Sonsini
Sen. Mark Hatfield (Oregon)

ACTEL
gross margin 56% of net revenues
small increase in FPGAs, but price erosion erased

ATMEL
gross margin = 74%
net revenues for logic up 40%
higher selling prices
logic is 7% of business
owns our fab

QUICKLOGIC
gross margin 60%
had fab runs with zero yield and low yields
market is telecom, video graphics, instrumentation,
high-end computing, military
litigation with Actel, lost with cross-licensing and payments result
and Unisys

QUICKSILVER
- target dynamic logic (real-time reconfigure) for multiprotocol
  - cell phones and roaming among protocols
- target DSPs [i.e. specialized uP]
- DSPs are dead
- bet that paging in logic (remotely) is less power and cheaper than
  - resident logic mostly idle
- bet HDLs need to convert to algorithm description C
- design for rapid partial configuration and background reconfiguration
- customize for single purpose, not general purpose prototyping
  - thus no generic overhead
- dynamic logic 10-50% power use of FPGA [wrong!, re CoolRunner]
  - and 10-100x faster than DSP [yes, but so is Xilinx FPGA]
- acknowledge acceptance problem, won't work until
  - there are sufficient engineers who understand the technology [!]

CHAMELEON
- target DSPs
- ASICs are dead
- 5-10x DSP performance
- claim stable timing for interconnect (MUX based)
- dynamic interconnect
- customized to single application
- architecture is reconfigurable uP with heavy hardware acceleration
- bet is software programmability (of hardware) is next big thing
  - just can't afford to wait for ASICs for any product
  - zero-time custom chips
  - IP cores as configuration bit-streams
  - customized IP cores in software
  - programmable logic and interconnect
  - pay reconfiguration overhead of CCA

MORPHICS
- target DSPs
- programmable heterogeneous uPs, i.e. many custom uPs

CRADLE
- generic scalable uP
- heavy data parallelism
- lots of uPs on one chip (20 RISC, 40 DSP, 5 DMA)

CLEARLOGIC
- fused crosspoints, no transistors [= Comesh]
- 72% less die than comparable CPLD
- zero added capacitance,
  - interconnect transistors always add power cost
- 33% less power
- typical interconnect puts 20 transistors on line

LIGHTSPEED

- mux-based interconnect and logic
- modular ASIC -- like sea-of-gates
- fast timing convergence during design (2 weeks) [!]
- minima for capacitance/resistance trade-off at 4um transistors
  - constant across architectures
  - low resistance = high capacitance and vice-versa
  - transistor size is fixed for interconnect and programmables
  - large part of custom design (and of Logical Effort)
- bet: no timing-driven software for programmable interconnect
  - and i/o pin locking problem kills large FPGAs

CRITICAL TECHNOLOGY WEAKNESSES (Comprehensive)

ASIC

- development time
- NRE costs
- no off-the-shelf parts
- design risk especially wrt time-to-market
- can't design in software
- can't update to new protocols or processes
- can't customize end system
- requires high volume
- no off-the-shelf substrate, supply issues

FPGA

- interconnect routing and loss of usable cells
- metastable timing wrt design changes
- unpredictable routing delays and logic capacity
- wasted interconnect (larger and slower)
  - 3x slower than ASIC/PLD, 10x larger die
- expensive design software, mandatory design software
- shortage of registers
- must complete design and place/route prior to knowing performance
- historically same software as ASICs

CPLD

- unpredictable logic capacity
- expensive design software, mandatory design software
- shortage of registers

SPLD

- gate count limitations
- fixed architecture
- extreme shortage of registers
- slow to reconfigure
- no partial reconfigure, no dynamic reconfigure

uP

fetching and decoding overhead
instruction set overhead
instruction set variability
slow bus interface
ALU operations cannot be customized
bit-width is fixed and often wasteful
no parallelism
cannot integrate peripheral processing
2-5% efficiency of ASIC
very inefficient resource usage, most logic elements are idle
e.g. adding two numbers uses 2% of CPU
rest of CPU is idle but still consuming power

SPLDs

Defacto industry standard SPLD: 22V10, 22-pins
12 dedicated inputs
product term array
product term allocation
10 macrocells
10 i/o cells

SPLD standards:
20 to 44-pins
100-1000 gates
2-level AND-OR logic
PAL = programmable AND, fixed OR, 1980 vintage
PLA = programmable AND, programmable OR
monolithic block-based structure
best PLD performance available

SPLD features
programmable i/o pins
flexible output-enable
bidirectional i/o
programmable output polarity
flexible register configurations
flexible clocking schemes

SPLD benefits
reduced power
faster turn-around
higher performance (due to reduced interconnect)
higher reliability
easy to use
easy to design with

easy to program
industry standard architecture
can specify with truth tables
logic minimization not necessary (er, impossible)

SPLD markets
all niche markets
simple embedded devices requiring low-cost and low-power
cellular phones, video games, hand-helds, notebook computers
other uses
disc drives, communication network hubs, bridgers, routers

Used extensively for decoding and simple state machines

CPLDs

CPLD market growth is in <25-50K as ASIC replacements

As CPLD size increases, they challenge ASIC designs of comparable size.
CPLDs are inherently faster than FPGAs for state machines

Migration from CPLDs to FPGAs
reduce PCB area
reduce power consumption (dated)
reduce cost
increase reliability (fewer components to integrate)
more portable products
overcome PLD gate limits

Migrate from PLDs to ASICs
when >10K units, NRE is covered
cheaper
faster
often want both off-shelf CPLD and ASIC version to manage market flows

FPGAs

sizes >100K gates *require* IP cores, including uP cores
Xilinx AllianceCORE
Altera Megafunctions Partners Program

IP cores are synthesized, thus easily customized in software

FPGAs are inherently faster than CPLDs for arithmetic

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Design time estimates and           logic utilization
      automated         several hours     50%
      interactive       1 day             75%
      manual            1 week            95%

Interconnect problems
      architecture trade-off
            cross-point = max flexibility, slowest, largest die
      difficulty increases as logic approaches saturation
      difficulty increases as pins become anchored
      after successful route and pinout, can't change design

One-hot FSM encoding is faster for FPGAs

Historically FPGAs are worse than CPLDs for
      FSMs
      counters
      complex arithmetic
and better for
      register-rich dataflow
but differences are disappearing


reconfigurability = cost of change = multiprotocol functionality
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