# LOSP SYNTHESIS SYSTEM:  VALUE PROPOSITIONS

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***ISSUE:***  Hardware design is costly, time-consuming, and difficult
***SOLUTION:***  Pragmatic benefits provided by a unified tool model

-- integrated verification prevents design change errors
-- incremental design development
-- faster time-to-market
-- fewer, faster design iterations
-- fewer design errors
-- controlled trade-off of key design parameters
-- cost savings and productivity gains
-- preserves reliability of delivery schedules


***ISSUE:***  New, larger designs press current tools to their limits
***SOLUTION:***  New synthesis capabilities

-- more efficient model of logic functionality
-- multilevel logic optimization
-- path optimization
-- partial simulation
-- logic/interconnect trade-off
-- comprehensive design coverage with fewer logic patterns
-- integrated front-end back-end tools and model
-- designs generated automatically to meet performance specifications


***ISSUE:***  Large designs are hard to manage and to modify
***SOLUTION:***  Powerful abstraction tools for management of complexity

-- hierarchical partitioning through-out
-- identification and abstraction of recurrent functional elements
-- bit-width abstraction
-- library module identification and extraction
-- parametric generator functions
-- control of critical path length
-- retiming and register relocation
-- design reuse and integration
-- identification and isolation of essential components
-- sequential/parallel decomposition
-- branching and path explosion management
-- structure sharing

*ISSUE:* Synthesis and design iteration require equivalence checking
*SOLUTION:* Built-in formal verification and goal-directed logic synthesis

-- redundancy and reconvergent path removal
-- false path identification
-- automated test pattern generation
-- automated test bench validation
-- correct by construction


*ISSUE:* Functional specifications are difficult to convert to hardware design
*SOLUTION:* Design space exploration tools guided by user goals

-- time/space trade-off
-- modular and localized design trade-offs
-- data path synthesis
-- top-down and bottom-up design
-- localized changes under parametric control
-- fan-in and fan-out control
-- pipelining
-- built-in formal verification


*ISSUE:* New tools require new skills
*SOLUTION:* Compatibility with standard design practices and tool chains

-- standard HDL and netlist input
-- netlist output at any stage of design
-- integrates with conventional tool chain whenever desired
-- handles all logic types with equal efficiency
-- handles all design types with equal efficiency