ILOC DEVELOPMENT OVERVIEW FOR DMC54

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We are benchmarking a commercial ASIC circuit design, DMC54, to compare the performance of ILOC to that of Synopsys. The circuit is a reverse-engineered custom DSP.

The strategy is to evaluate ILOC in small steps as we refine it toward a commercial tool for ASIC optimization. Simple metrics used to measure ILOC performance are reported here, and are rounded to reflect measurement accuracy.

DMC54

DMC54 is an excellent design to work with. The registers have been removed so that the design is purely combinational. Some initial measurements:

Inputs/outputs:	77/41
TSMC cell types:	40
TSMC cells:	4422
Internal pins:	8463
Internal nets:	4831
2NAND gates:	5206
Greatest fanout:	48
Critical 2NAND path:	103

PRELIMINARY ILOC OPTIMIZATION

A quick analysis and optimization with no refinements yields:

		% Reduction
Internal pins:	6182	27%
Internal nets:	3841	20%
2NAND gates:	4132	21%
Critical 2NAND path:	72	30%

These results are consistent with results on all other benchmarks. No measurements have been made yet for TSCM cells, or for critical path dynamic timing.

Caution: this analysis uses the ILOC internal unit counting metrics, and does not reflect a competitive evaluation.

The preliminary optimization was mapped into CoMesh:

CoMesh blocks:	52		
CoMesh area (.18u):	4.7 mm^2		
CoMesh timing:	3.3ns	=	300 MHz
CoMesh pipeline set-up delay:	36ns		
CoMesh timing improvement	200%	(Synopsis reports 6.7ns)	
CoMesh area cost:	120x	(~ASIC area = .04 mm^2)	

ASIC area is roughly estimated as (2NAND-area * #-2NAND-gates * 2). The CoMesh area uses a factor of 2x for routing, so again we see that bringing the routing factor down to between 1x to 1.5x is necessary for a reasonable area ratio to ASICs. (1x routing gives a 78x area ratio to ASICs.)

ASIC delay expressed as 2NAND gates (critical path = 72) is

2.4ns + wiring delay

No critical path optimization has been performed. The critical path length will also definitely decrease when we map to TSMC cells.

SOFTWARE STATUS

Prior to providing an ILOC-reduced version of DMC54 for Synopsis timing analysis, it is appropriate to do some work on critical path reduction. These algorithms need to be written:

- Smarter technology mapping to fast TSCM cells
- Unit delay path optimization
  - Find critical paths
  - Find optimal reduction points
  - Reduce critical paths
- Manage fanout and network topology

I'll also generate Verilog files for before and after optimization for several circuits in our benchmark set, in order to test Synopsis behavior on a diversity of circuit topologies, particularly those that are difficult to place and route.

The next steps in path optimization require much more sophisticated propagation models:

- Generalize ILOC simulator for dynamic timing analysis
- Model electrical loads over network topology and branching
- Model path delays through gates and wires
- Balance path delays across network

Model RC and parasitic delays in wires
Combine all models to provide a general interactional model of delay
logical + topology + electrical + parasitic delay effects
Extend optimization tools for each model

OVERVIEW, JUNE 2003

We are comparing ILOC performance to that of Synopsys for the same designs, while using Synopsys to provide accurate timing and area accounting. ILOC provides a ~30% reduction in design size, but at the cost of very slow timing. It is apparent that ILOC needs a timing and capacitance model in order to address timing during the optimization process. We are currently building that model. Part of the testing will be to get fair comparisons of concurrent timing and area optimization.

Expectations

The expectation for near-term ILOC development should be:

1. Competitive adequacy: we can do what the competition can do.

2. Minor improvement from partial solutions: by doing 70% of what others do, we can gain minor (5-10%) improvements for ASIC optimization when both area and timing are considered. Doing the other 30% will yield major improvements (15-25%) after significant development effort.

Lessons Learned

There are several consistent lessons learned coming from work with commercial designs. The partial conclusions listed below are ordered from "good news" to "bad news":

1. Commercial designs are almost identical to the 200 academic benchmarks used to ground ILOC performance over the last decade.

2. ILOC area optimization (without concern for timing) is the same for all designs, on average around 20-25%.

3. Iconic logic provides exceptional capabilities for design analysis, including many tools that do not exist in other commercial products (such as top-down and bottom-up visualization and abstraction, complexity analysis, and localized goal-directed transformation).

4. ILOC does not as yet provide several necessary conventional tools, especially timing analysis. Iconic logic does include a rather revolutionary

model of timing performance that permits, for example, design of new types of flip-flops, new hardware (eg CoMesh), and new asynchronous and parallel models. What it does not yet provide is conventional tools for conventional architectures. These need to be developed. There are no inherent difficulties or complexities here other than investment of time and resources.

5. The ILOC code has become quite brittle, making it difficult to extend to new capabilities. The cost is in development time and effort, not in native capabilities. This can be completely remediated by a code rewrite.

6. Development of conventional tools (such as an FPGA mapper and a timing model) will require significant careful effort; there is no "magic bullet" that lets ILOC solve significant optimization problems quickly and easily. Iconic logic should be viewed as a more efficient hammer for conventional nails, and not as an electronic nail gun.

7. All conventional optimization problems are very difficult (exponential). There is no free lunch. Commercial software tools are quite good and are the result of decades of development by dozens of skilled people. 90% of the extension of ILOC is simply specialized technical details that provide no technical challenges but require significant development effort.

8. For ILOC to be competitive, it must include all the internal optimization and modeling features of current commercial tools. ILOC will not show its full potential in the quick and partial tools we are currently developing.