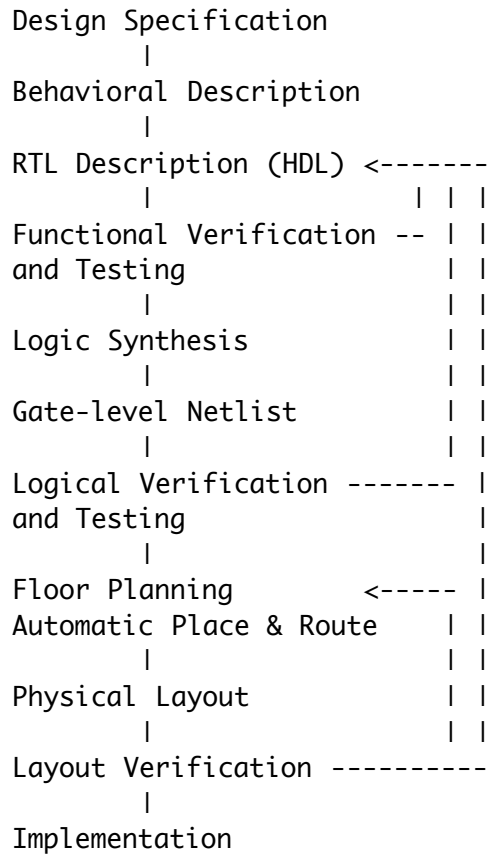
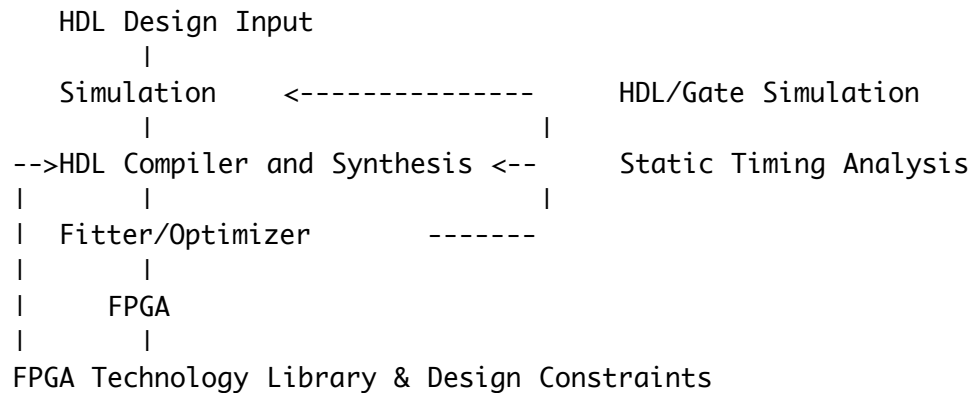


SOME DESIGN FLOWS
William Bricken
January 2002

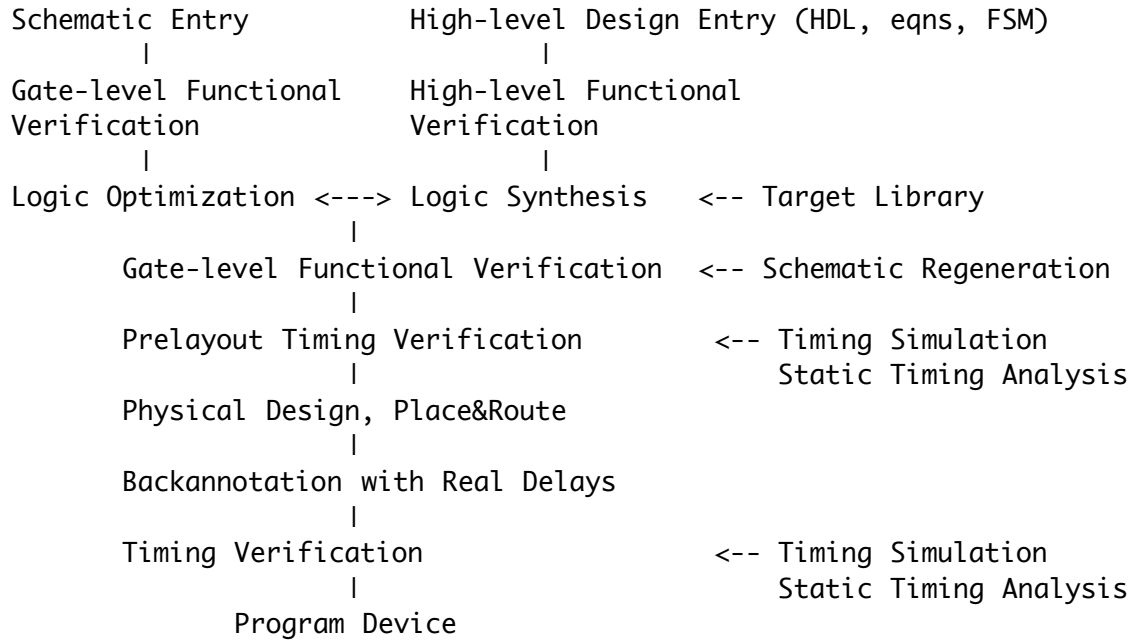
GENERIC



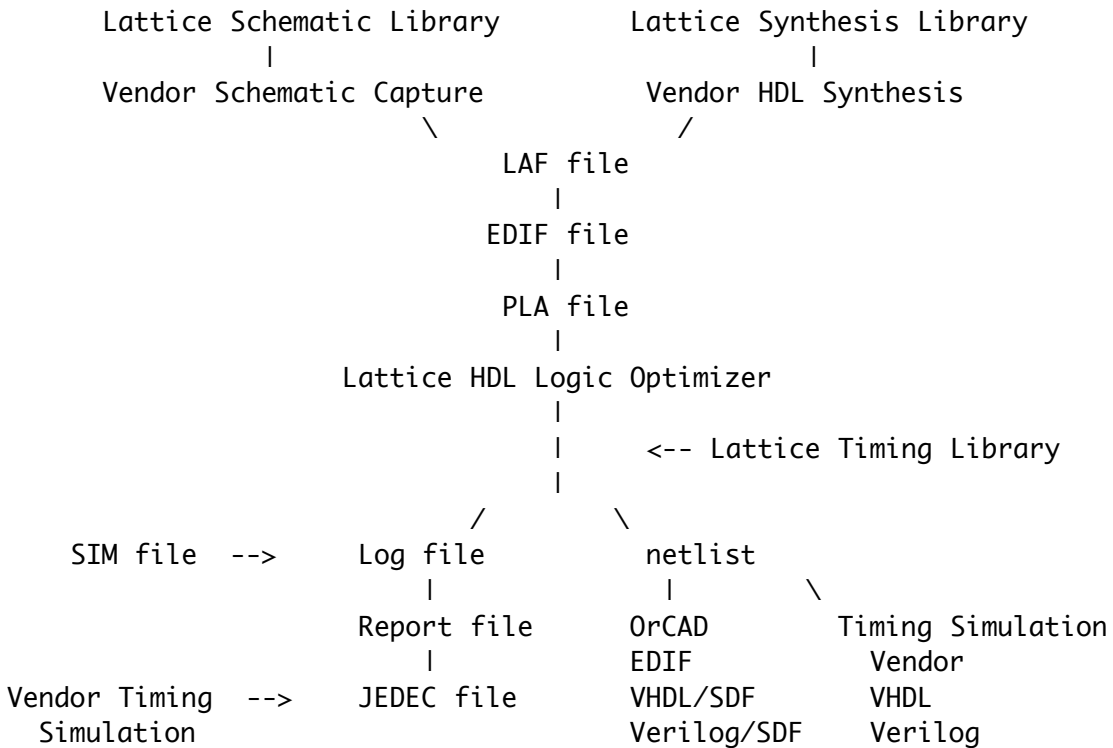
FPGA



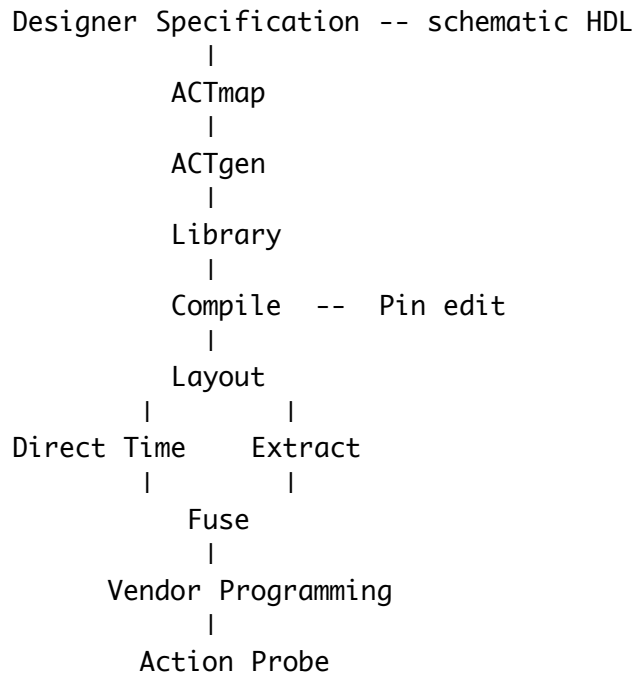
STANDARD CONVERGENT



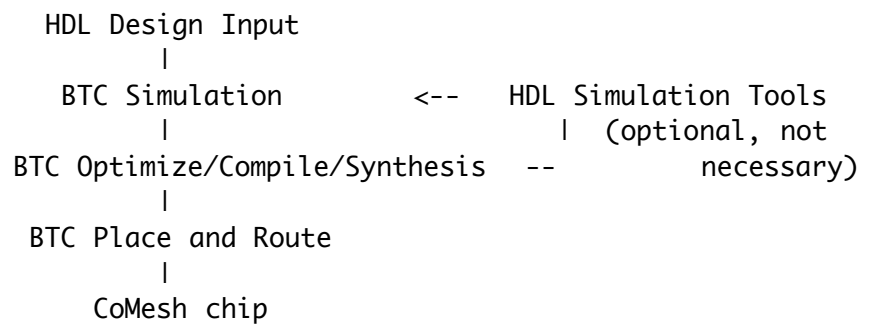
LATTICE



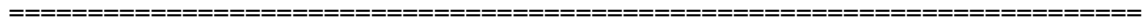
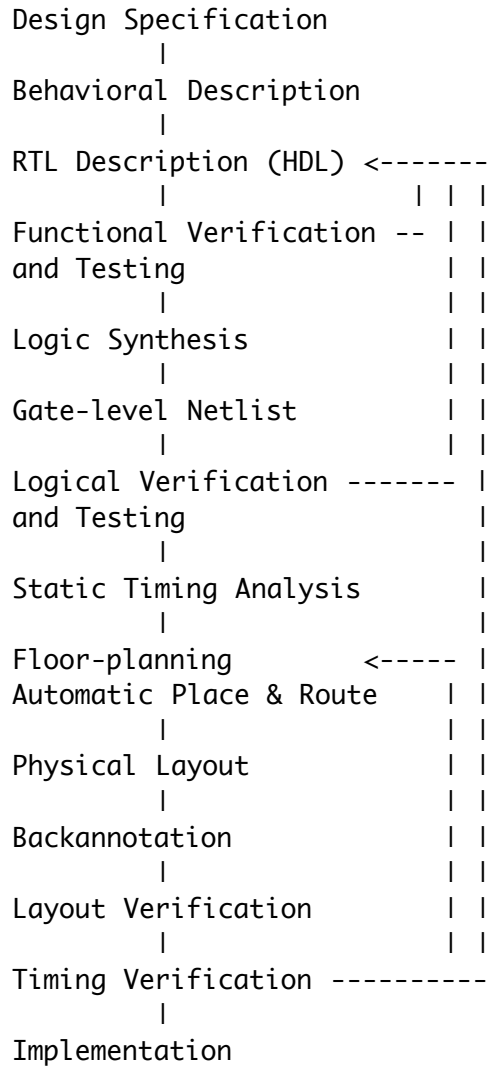
ACTEL



COMESH



HYBRID



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COMPARE GENERIC TO COMESH

Generic Design Steps

BTC Design Steps

Device Selection			select CoMesh	
Design Specification			same	
Behavioral Description			same	
RTL Description (HDL) <-----			untimed HDL, FSM or Boolean equations	
Functional Verification --			BTC functional simulation	
and Testing				
				single step
Logic Synthesis			BTC Synthesis and Optimization	
Gate-level Netlist			available on demand	
Logical Verification -----			BTC Formal Verification	
and Testing				
Technology Library Map			available on demand	
Prelayout Timing			not required	
			(or technology specific)	
Floor Planning <-----			not required	
Automatic Place & Route			(or technology specific)	
Physical Layout			CoMesh configuration	
			(or technology specific)	
Delay Backannotation			available on demand	
Timing Verification			CoMesh Timing Verification	
			(or technology specific)	
Layout Verification -----			CoMesh Verification	
			(or technology specific)	
				single step
Program Device				