CRITICAL TECHNOLOGY WEAKNESSES

William Bricken
November 2002

ASIC
- development time
- NRE costs
- no off-the-shelf parts
- design risk especially wrt time-to-market
- can't design in software
- can't update to new protocols or processes
- can't customize end system
- requires high volume
- no off-the-shelf substrate, supply issues

FPGA
- interconnect routing and loss of usable cells
- metastable timing wrt design changes
- unpredictable routing delays and logic capacity
- wasted interconnect (larger and slower)
  - 3x slower than ASIC/PLD, 10x larger die
- expensive design software, mandatory design software
- shortage of registers
- must complete design and place/route prior to knowing performance
- historically same software as ASICs

CPLD
- unpredictable logic capacity
- expensive design software, mandatory design software
- shortage of registers

SPLD
- gate count limitations
- fixed architecture
- extreme shortage of registers
- slow to reconfigure
- no partial reconfigure, no dynamic reconfigure

uP
- fetching and decoding overhead
- instruction set overhead
- instruction set variability
- slow bus interface
- ALU operations hard to customize
- bit-width is fixed and often wasteful
- no parallelism
- cannot integrate peripheral processing
- 2-5% efficiency of ASIC
- very inefficient resource usage, most logic elements are idle
  - e.g. adding two numbers uses 2% of CPU
  - rest of CPU is idle but still consuming power