Bricken Technologies

Iconic Array™ Hardware Virtual Structure:
Lowest Logic Latency, Unmatched Flexibility

Bricken™ Technologies is developing a radical solution to the problems of semiconductor physical design complexity: the *Hardware Virtual Structure.* BTC's patent-pending Iconic Array™ HVS is hardware that behaves like software: instantly programmable with unmatched flexibility.

Iconic Array™ HVS: A Truly Different Technology

BTC's Iconic Array™ HVS has the flexibility of software programmability while providing hardware performance. Like a microprocessor, the HVS is a computational structure, its behavior is specified dynamically by software. As an integrated circuit, the HVS is implemented with all the benefits of hardware parallelism. Thus the HVS combines the best of two worlds, *structural flexibility with ASIC performance*.

The HVS is fully programmable, yet it requires no "traditional" placement and routing. Instead, the HVS hardware partitions its own resources based on a netlist (a specification of gates and connecting wires), making both timing and wiring virtual rather than physical, software rather than hardware.

Unlike other programmable and reconfigurable devices, the Iconic Array™ programming is derived directly from a Hardware Definition Language functional specification. The untimed synthesizable subset of Verilog is sufficient; in fact, any formal specification will do.

Using immediately available software provided by BTC, the untimed synthesizable Verilog specification (or netlist) is then optimized, verified, and translated into the programming that determines the operation of the Iconic Array™ HVS. It takes just a few minutes to generate HVS programming for a 5000 gate circuit.

The Iconic Array™ programming is not comprised of a sequence of instructions, but of bits representing the desired functionality using Iconic™ Logic, a fundamentally new approach to logic that is the foundation of BTC's proprietary hardware and software.

As a first approximation, the Iconic Array™ HVS is comprised of:

1. A memory-like substrate similar to DRAM, with equivalent cost of fabrication.
2. A Logic Supervisor ™ This computational engine does not resemble a CPU or a DSP or a FPGA; it is a fundamentally new technology built on Iconic™ Logic. The engine can run at gigahertz rates, and takes four clock phases to evaluate any combinatorial function, *independent of complexity*. For sequential circuits, the engine is a pipeline with four clock phases between registers, again independent of the complexity of the logic between the registers.

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3. Iconic Array™ software loads the data structure defined by the functional design and programs the Logic Supervisor™. This software is written into the device, with the same efficiencies of writing into and reading any memory. Because the functionality itself is simply represented by a static array of bits in memory, the HVS can be dynamically reprogrammed to perform different functions at memory speeds. Since Iconic Array™ software files are relatively large, we are boosting logic performance using inherently faster memory technology.
4. Proprietary Algorithms. BTC's Iconic Array™ logic reduction paradigm, implemented in silicon, makes use of registered inputs applied to a programmable data structure to produce fast, efficient outputs with uniform delays. Performance is determined by the Iconic Array™ hardware, which is free of path delays introduced by place and route software. The result is uniformly minimal logic latencies across all paths – not just those designated critical .

Unique Capabilities And Benefits

The capabilities of the Iconic Array™ HVS will have a significant impact on the design, performance, and cost of synthesized logic designs:

- Design effort is streamlined since timing delays are not exacerbated by traditional place and route issues.
- Substantial Non-Recurring Engineering (NRE) costs are eliminated when Iconic Array™ HVSs are used as ASIC substitutes.
- Since there are far fewer steps in HVS partitioning, verification is simpler.
- Improvements in fabrication techniques accrue for the HVS more rapidly than for other technologies. Increases in gate count and density, reduced die sizes, and increased clock speeds all directly improve the performance of the Iconic Array™ HVS. DRAM density, and thus HVS capability, is increasing faster than other technologies.
- Since wiring is virtual, deep submicron design issues for complex circuitry are muted.
- The Iconic™ Logic synthesis and optimization algorithms used in HVS configuration outperform all other commercial synthesis technologies.

Most Efficient Time-To-Market

To repeat: the HVS provides both timing and routing for any synthesizable Verilog specification or netlist. Design issues associated with timing and wiring are no longer pivotal. Since the Iconic Array™ software takes industry standard HDL files as input, there are no new design skills or techniques to learn. Iconic Array™ software files are generated in minutes. Once the desired functionality is specified in HDL, a hardware implementation can be operational with a simple download. These capabilities add up to a fundamental change in semiconductor design practices: *Guaranteed minimum design latency.*