PROBLEMS SOLVED UNIQUELY BY BTC PRODUCTS

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Lower Cost Of Ownership

ISSUE: Routing congestion wastes logic resources and degrades timing performance
SOLUTION: Superior functionality
- 300 MHz guaranteed for five levels of logic
- automated synthesis/place&route turn-around within hours
- integrated verification to reduce risk in design changes

ISSUE: FPGA architectures have too little logic, too much routing
SOLUTION: More user logic resources for the same cost
- easier and less expensive design integration
- more efficient synthesis and layout for better resource utilization
- sufficient available logic to accommodate almost any user design

Faster Time-To-Market

ISSUE: Design iterations change timing performance, requiring complete redesign
SOLUTION: Fewer, faster design iterations
- automated timing closure
- stable timing behavior even as the design changes
- integrated verification prevents design change errors
- preserves reliability of delivery schedules

ISSUE: Changing designs is difficult, time consuming, and introduces errors
SOLUTION: Fewer engineering hours to reach design goals
- incremental design development
- automated test bench validation
- complete, one-step integrated tool chain
  from functional verification to functioning hardware

Superior Ease-Of-Use

ISSUE: Good design takes too much time, too much expertise
SOLUTION: Automated circuit generation, synthesis, placement and routing
- designs generated automatically from functional specification
- designs generated automatically to meet performance specifications
- no additional hand crafted layout work
- no specialized hardware expertise required
- up to 50% reduction in logic for given functionality

ISSUE: Customers don't want to learn new skills, techniques, or systems
SOLUTION: Backwards compatibility to all standard tools
- HDL or netlist in - netlist out
- integrates with conventional tool chain whenever desired
- handles all types of logic with equal efficiency
- locked-down pin assignment does not affect timing or logic capacity
- pin-compatible products

ISSUE: EDA software and FPGA hardware are supported by different companies, lack integration
SOLUTION: Superb engineering support
- easier trouble-shooting because of hardware/software co-design
- readily available standard parts, rapid product delivery

ISSUE: Support of industry standard protocols and capabilities
SOLUTION: Included on the chip are
- eight or more clock domains
- internal diagnostics and debugging
- compliant to PCI and other bus protocols
- compliant for almost all i/o protocols and standards
- wide diversity of available IP cores