ILOC/SYNOPSYS COMPARISON PROJECT -- DESIGN DESCRIPTIONS

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October 2003

Ten combinational designs from the ISCAS/MCNC benchmark suites were selected for the performance comparison study between ILOC and Synopsys. A brief description of these designs follows. The extent of design description varies in accordance with available information.

BRIEF SUMMARY STATISTICS

ILOC measures for the unoptimized golden version of each circuit follow.

Name	I/O	GATES	NETS	AREA	DELAY
CM85A	11/3	44	88	780	1349
MAJTAUT	44/1	155	150	1495	1213
C432	36/7	212	355	3338	3782
9SYMML	9/1	222	159	2184	2021
C1355	41/32	518	949	9213	3705
TABLE5	17/15	1180	718	10738	2008
C5315	178/123	1926	3101	30132	5987
C7552	207/107	2238	4343	40549	7075
CORDIC	23/2	2890	2079	29578	2475
TOO_LARGE	38/3	14490	1111	87562	18623

GATES counts two-input simple logic gates, inverters are not counted.

NETS counts all wire nets between primary inputs, internal gates, and primary outputs.

AREA and DELAY are measured by the ILOC model. Area is in square microns; delay is in picoseconds.

CM85A

CM85A is a 4-bit magnitude comparator with three enables. Three mutually exclusive outputs indicate the comparison between two four bit inputs:

```
in[3:0] EQUAL-TO     in[7:4]
in[3:0] GREATER-THAN in[7:4]
in[3:0] LESS-THAN    in[7:4]
```

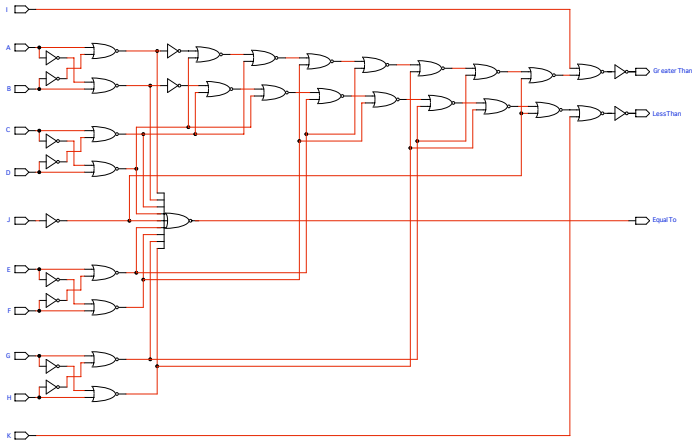
There is a one-bit enable for each of the three outputs, permitting comparators to be ganged together to generate comparisons between wider bit-width inputs.

Structure

Two long NAND chains mix the results of XORing each bit pair being compared. The EQUAL test is a mix of the four XOR tests.

CM85A is small design, supposedly with a known minimum. However, the conventional magnitude comparator has separate subcircuits for <, =, and >. It is possible to use the orthogonality of the outputs <, =, and > to express one of them in terms of the other two, potentially generating a smaller design. ILOC can use its built-in theorem prover to guide design using semantic information. Gains get multiplied by bit-widths. This 4-bit comparator may show a small gain, while the reduction of a 16-bit or 32-bit comparator would show proportionally larger gains.

Schematic



Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD	44	88	780	1349
ILOC	35	75	472	368

MAJTAUT

MAJTAUT is a composite of a simple 3-out-of-5 majority circuit, confounded by the inline incorporation of five different tautologies. Only 5 of the 44 inputs are relevant to the single output.

Each tautology has no effect on the output of the circuit. A reduction engine should identify all five and delete them. None are essentially difficult or large.

Structure

The 3/5 majority circuit consists of 9 gates. Added tautologies:

TAUTOLOGY 1: A Boolean factoring problem from Haectel
7 inputs in 13 clauses -- 29 gates

TAUTOLOGY 2: Distribution of IF-THEN-ELSE from McCarthy
5 inputs in 4 nested MUXes -- 19 gates

TAUTOLOGY 3: A constructed equivalence that uses advanced features of ILOC reduction to reduce directly.
8 inputs nested in 6 logic stages -- 22 gates

TAUTOLOGY 4: The 3/2 pigeon-hole problem
6 inputs in 14 clauses -- 30 gates

TAUTOLOGY 5: Three-coloring a tetrahedron
12 inputs in 34 clauses -- 46 gates

Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD	155	150	1495	1213
ILOC	9	18	102	223

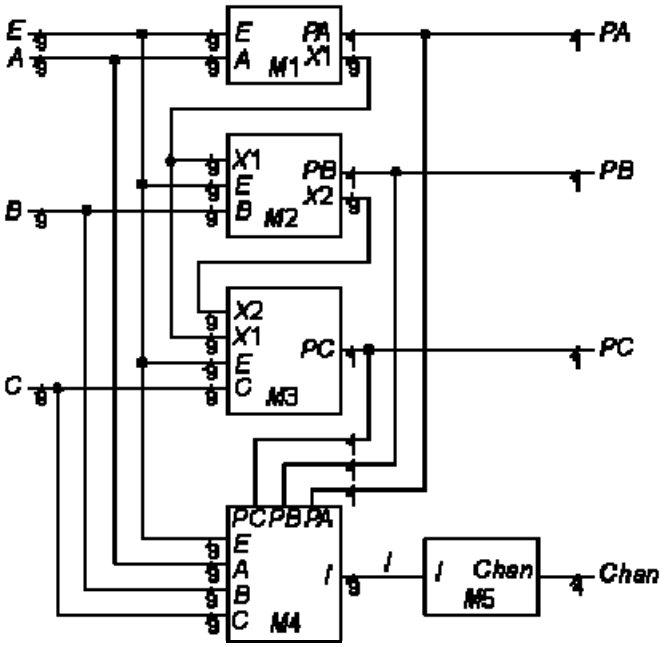
C432

C432 is a 27-channel interrupt controller. 36 inputs are grouped into four 9-bit buses; three buses carry the interrupt requests, and the fourth enables and disables the requests. The seven outputs specify which channels have acknowledged interrupt requests.

Structure

C432 is highly structured, replicating its underlying logic across 9-bit vectors. Finding the best partitioning across the many structural perspectives is difficult; there are lots of potentially wasteful traps using the wrong XOR and MUX gates. It is easy to get the first 80% of reduction, not easy to get the rest.

Schematic



Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD	212	335	3338	3782
ILOC	176	189	1660	2120

9SYMML

9symml counts ones in a 9-bit input, the single output indicates exactly 2 or 7 ones. The benchmarks include two versions of this circuit. 9SYMML is a multilevel logic version that has a smaller area, while 9SYM is a flattened version with lower delay.

Structure

9SYMML has very little internal structure, with only a few XORs and MUXes. ILOC can find little to reduce, although delay can be significantly improved.

Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD-9SYM	395	154	3740	1598
GOLD-9SYMML	222	159	2184	2021
ILOC	201	223	1770	796

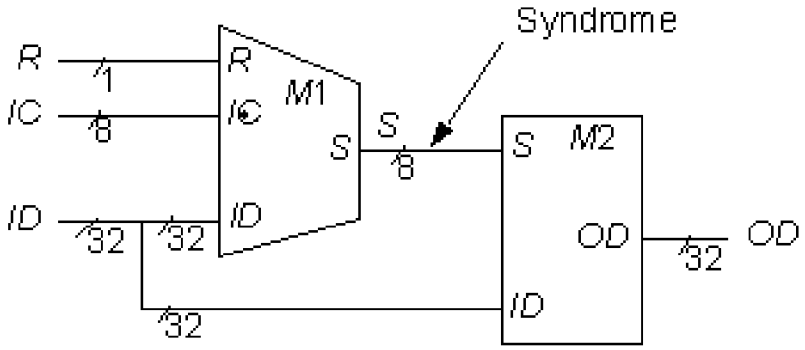
C1355

C1355 is a 32-bit single-error-correcting circuit. 41 inputs combine to form an 8-bit internal bus, which then combines with 32 primary inputs to form 32 outputs. The syndrome S is a (40,32) Hamming code. The benchmarks include two versions, C499 is expressed using XORs and MUXes, while C1355 maps the functionality onto only simple gates.

Structure

The syndrome consists of eight Boolean equations that use XORs extensively to compare bits, thus XORs dominate the design. Almost all of the 32 outputs have the same length critical path, so the network acts quite globally, with little localizable waste. There are two challenges: wasted area associated with premature commitment to nested XORs, and finding the NAND partition that makes all cells small.

Schematic



Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD	518	949	9213	3705
ILOC	504	205	3452	1475

TABLE5

Table5 is a look-up table that defines a function expressed in the form of Boolean clauses. The particular function is designed to be difficult to minimize. Look-up tables are widely used for top-level specification of behavior during design. They are common in silicon for many functions that in general require more effort to compute than to look-up, examples are trigonometric functions, hyperbolic functions, and some filters.

Structure

Look-up tables convert to a very clumsy and wasteful network specification. Thus they require extensive logic optimization. TABLE5 has very little structure that conveniently reduces; it is rather like glue logic, having no particular structure, no module replications, no XORs or MUXes, and no regular structure to aid optimization.

Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD	1180	718	10738	2008
ILOC	605	606	5148	1369

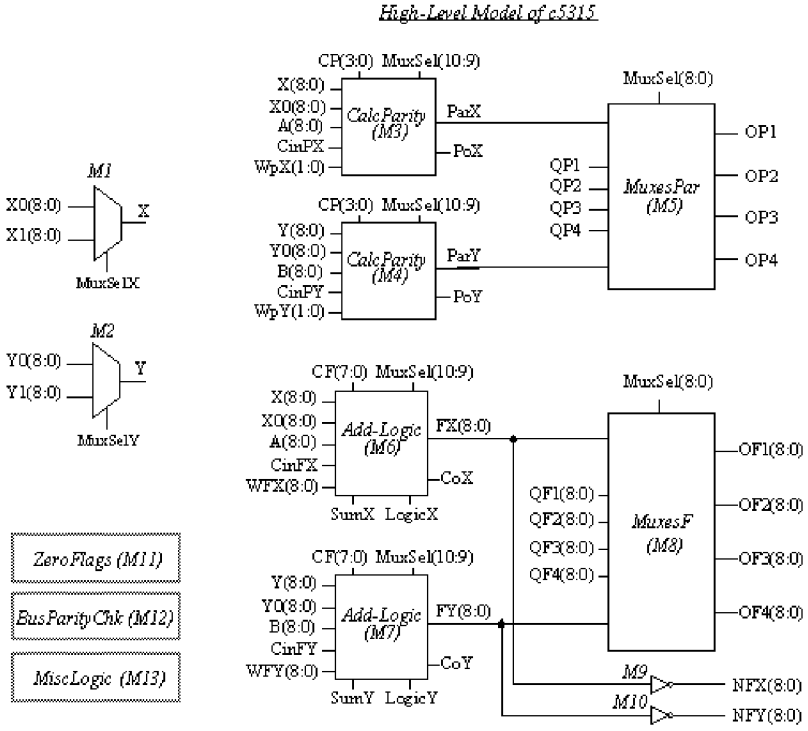
C5315

C5315 is a 9-bit ALU that performs arithmetic and logic operations simultaneously on two 9-bit input data words, and also computes the parity of the results. Arithmetic and logic operations are specified by an 8-bit control input bus. The circuit also includes logic for calculating various zero and parity flags of the input buses.

Structure

Modules within C5315 include two identical 9-bit carry-select adders, a 9-bit sum parity checker, a logic block that computes all 16 of the two-input logic functions, a 9-bit logic parity checker, a 9-bit bus parity checker, and MUX logic to steer results to appropriate outputs. Thus the design consists of a large proportion (~70%) of XORs and MUXes.

Schematic



Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD	1926	3101	30132	5987
ILOC	1473	1630	13935	2683
SYNOP	1611	1770	14051	2923
ILOC-REDO	1361	1916	12247	2368

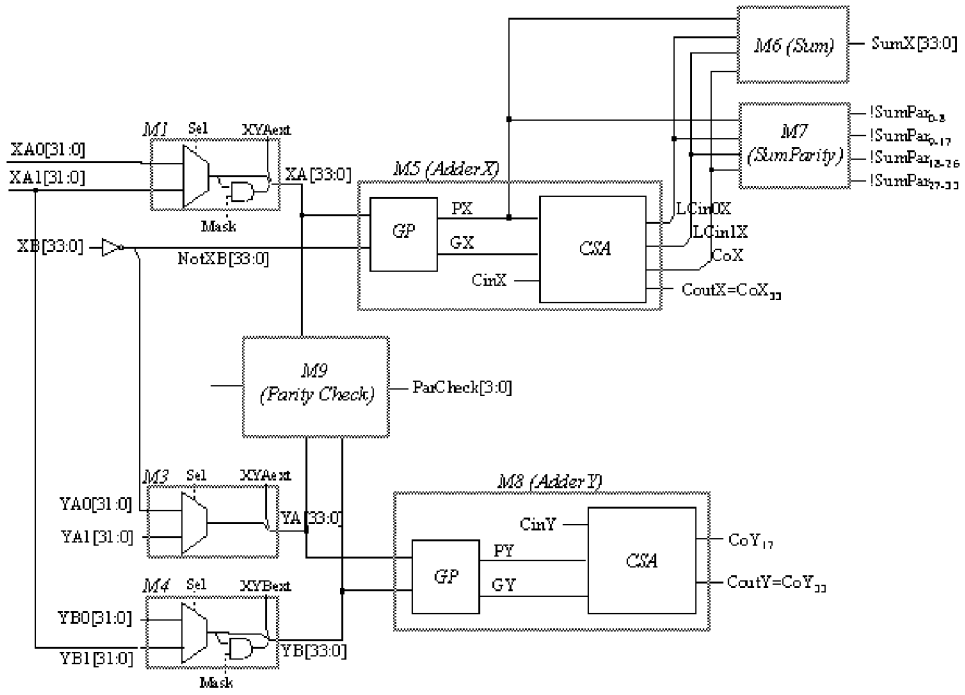
C7552

C7552 is a 34-bit adder and magnitude comparator with input parity checking.

Structure

The two internal adders are 34-bit carry-select adders consisting of alternating 4- and 5-bit blocks. The 34-bit comparator has an output for the whole 34-bit inputs as well as for the 17-bit portion of the inputs. The 34-bit parity checker calculates the parity for four partitions of the adder output.

Schematic



Performance:	GATES	NETS	u^2 AREA	ps DELAY	
GOLD	2238	4343	40549	7075	
ILOC-AREA1	1586	1900	14226	5035	-- area emphasis, no delay
ILOC-AREA2	1656	1693	15676	2579	-- mixed area and delay
ILOC-AREA3	1656	1693	16658	2210	-- delay emphasis, minor area

CORDIC

CORDIC stands for COrdinate Rotation DIgital Computer, it is a shift-add algorithm for rotating vectors in a plane. It is used extensively for computing trigonometry functions and in Fourier transforms.

Structure

The golden version is excessively inflated in area due to PLA flattening. Although the PLA should be faster, the capacitance effects due to very large fanout slows the circuit more than a multilevel version. Careful selection of nested logic improves both the area and the delay.

Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD	2890	2079	29578	2475
ILOC	74	104	678	870
SYNOP	171	202	1776	991
ILOC-REDO	108	174	1153	658

TOO_LARGE

TOO_LARGE is a mapping of a function to an FPGA. The mapping is pathological, requiring too much fanin in the flattened format. There are very large fanin OR gates with inputs of 264, 278, and 533.

Structure

Careful collection of shared terms during logic deepening significantly reduces this design.

Performance:	GATES	NETS	u^2 AREA	ps DELAY
GOLD	14490	1111	87562	18623
ILOC	479	771	4366	1358