ILOC LOGIC REDUCTION and COMESH LAYOUT for THE SP700 DESIGN

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The objective of this project is to evaluate the performance of the ILOC software and the CoMesh hardware architecture using a specific commercial design, SP700. ILOC is a proprietary circuit design analysis and optimization engine based on novel mathematical techniques. CoMesh is a reconfigurable silicon architecture custom designed for ILOC capabilities. Results are reported for software and for hardware separately. This technical report contains an Executive Summary, a Technical Discussion and an Appendix that includes detailed statistics.

EXECUTIVE SUMMARY

CONCLUSIONS

When measured by the number of standard two-input logic gates, the ILOC software reduces the structural VHDL netlist by 25%. The critical path length of 75% of all submodules decreased as a result of logic minimization.

When mapped onto a four-input LUT architecture, the ILOC reduction is highly sensitive to optimization goals. Current algorithms focus on routing rather than logic reduction. ILOC LUT mapping does not reduce the raw number of LUTs compared to the LUT map generated by the Synplicity software, the ILOC mapping does however reduce the routing required by the LUTs by over 35%. As well, the critical path length of 70% of all submodules decreased. The ILOC LUT mapping algorithms lack the customization specific to the Virtex architecture incorporated in the Synplicity software.

When mapped onto the CoMesh architecture, the entire design can be implemented in a logic fabric area of approximately 111 mm^2 (.13 process geometry), with an expected pipelined cycle time of 180 MHz.

The SP700 design analysis is proof in principle that ILOC can be applied to complex commercial designs. The analysis falls short, however, in providing clearly interpretable results upon which to base business decisions. A more rigorous design methodology and process is currently being developed.

SUMMARY OF RESULTS

Results are reported for two top-level SP700 modules (SAMMEL_SPS and ARITHM). The two modules represent over one-third of the total design; SAMMEL_SPS is a small module covering 2% of the design, while ARITHM is the largest module in the design, consisting of 36% of the entire design.

Software

The two modules represent approximately 70K two-input ASIC logic gates, and are reduced using ILOC algorithms to approximately 52K gates of the same type, *a logic reduction of 25%*. These modules incorporate approximately 2000 registers that are not included in this gate count. Path length reduction varied widely over submodules, from -20% to +24%. In cases of increased path length accompanied by logic reduction, a space/time trade-off choice is possible. Further, applying ILOC path reduction tools to the longest critical path can be applied to reduce the path length to a desired delay, with an accompanying increase in logic area.

To more accurately convey the performance of ILOC algorithms, ILOC settings and parameters were not customized for any particular submodules. In a real-world design environment, a designer may specify different parameters for different parts of the design, emphasizing reduction of path length, for example, along the critical path, while emphasizing area conservation along non-critical paths. By design iteration using different ILOC parameters, almost all particular results can be improved. The *overall average results* show substantial overall average logic reduction across the entire design. Specific results are in the Appendix.

The two analyzed modules require about 15K four-input look-up tables (4LUTs). When logic is mapped into 4LUTs without consideration of wiring requirements, ILOC increases the number of required 4LUTs by 2% compared to the Synplicity log. However, this increase in raw LUT count is accompanied by a conversion of many 4LUTs into 2LUTs and 3LUTs, thus reducing the wires required to route the design. When LUT mapping is weighted using the Synplicity gate counting metric, ILOC reduces the design complexity by 37%. Along with the logic reduction, the critical path length of 70% of the submodules decreased; the critical 4LUT path length reduction varied from -39% to +64%. Again, in cases of increased path length accompanied by logic reduction, a space/time trade-off choice is possible.

LUT mapping results are from simple LUT-mapping algorithm written especially for this report. LUT results do not reflect ILOC capabilities. For example, the LUT-mapper does not use the supporting logic found in Virtex chips, such as carry-chains. As well, ILOC currently separates reset and enable logic embedded in LUT registers. In comparing LUT metrics to the Synplicity log, ILOC results are adjusted for both register and non-LUT support logic. Adjustments are needed only for the LUT technology mapping comparisons. We is currently preparing a suggested methodology for making fair LUT-based comparisons of ILOC and Synplicity performance.

Silicon

A .13u CoMesh block uses .05 mm^2 of silicon for reconfigurable logic and supporting global routing. The two SP700 modules require 740 CoMesh blocks, a total silicon area for logic and routing of 37 mm^2. The overall chip logic density after placement and routing of the design modules is greater than 2500 gates per mm^2.

The CoMesh silicon architecture bears almost no resemblance to the LUT-based architecture of the original design. Each CoMesh block includes pipeline and storage registers as well as five levels of logic, while ILOC software completely retimes the design to fit the pipeline. The CoMesh design is intended to solve the performance problems of current LUT-based FPGAs.