MODELS OF CIRCUIT PROPERTIES in LOSP

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Parens and pun notations for boundary logic provide a unified framework for modeling many aspects of circuit performance and design. This memo lists the mappings between measurement of formal aspects of a parens representation of a circuit and measurements of physical behavior in circuitry .

Aspect: ***Functional Behavior***

Specification languages for input include propositional logic, Boolean algebra, FSM state transition tables, and edif netlists. Logical functionality is treated as a global invariant for all other transformations.

Aspect: ***Transistor Area***

Modeled as the number of literals mentioned across all nodes of the graph; that is, the count of the number of inputs to all gates. In parens, count each literal and each bound once. To reduce transistor area, 1) reduce the number of literals through Extract and Distribute, and 2) Coalesce multiple references (Coalesce increases fanout and adds timing dependencies).

Aspect: ***Combinational Logic Propagation Time*** (aka delay, critical path)

Modeled as the greatest number of gates through which an arbitrary input vector must pass to generate the output. The longest topological path is an upper bound, but it could be "false", that is, never activated. In parens, the deepest recursive call to the fast satisfiability algorithm measures the delay. Also the greatest number of passes of the Losp bit encoded stack machine. The only circumstances in which the topological path is not the critical path is when a circuit has reconvergent fanout, caused either by redundant wiring, by branches in logic, or by coalesced circuitry. Redundancy is largely removed by the Insert algorithm. Coalescing is either postponed until a latter step in processing, or done when the abstracted subgraph is expected to be persistent.

Aspect: ***Wiring Metrics***

Modeled as the number of variable references across all nodes of a graph, that is the number of inputs to all gates. In parens, the count of variable references plus boundary references. Wire density is most influenced by factoring, that is by isolating subgraphs and removing symmetries over multiple references.

Aspect: ***Fanin and Fanout***

Modeled as the number of inputs (either literals or subgraphs) to each gate, and the number of outputs, respectively. In parens, fanin is the count of members of each boundary, while fanout is the count of members of each

boundary in the inverse graph. The inverse graph specifies the back links up the parens form created by multiple reference to literals and subgraphs. It can be visualized as signals traveling backward through the circuit. To conform to a maximum fanin (or fanout) restriction, groupings of the permitted size are isolated by a nested OR gate.

Aspect: ***Structure Sharing*** *(coalesce)*

Modeled by fanout from graph nodes. In pun form, the construction of a labeled pun cell. The label is then used for multiple reference to the cell/subgraph. Coalesce is best applied after all reduction and standardization techniques.

Aspect: ***Power Consumption***

Modeled as the number of transistor transitions during a single cycle of processing an input vector into an output vector. Transitions obviously depend on current circuit state, that is on the residual gate states from the previous input vector. In parens, the count of the differences in boundary crossings for two successive evaluation vectors.

Aspect: ***Noise during Operation***

Modeled as the number of concurrent crossings during traversal of a boundary graph. In parens, the count of the number of reductions on a single pass of the bit encoded stack machine, or as the count of potentially parallel reductions at an arbitrary tick of processing time. Transforms that impact timing (such as Distribution, factoring, and Coalescing) also effect noise.

Aspect: ***N-LUT Mapping***

Modeled as Boolean functions of n variables, connected in a regular network. In parens, groupings of N variables within an outer boundary, and without regard to inner boundary structure. Structural transformations which change the number of variable references access a search space for alternative mappings.

Aspect: ***Pipelined Logic***

Modeled as a collection of subgraphs, connected hierarchically, with a common maximum propagation delay. In parens, forms with equal critical path lengths (topologically and naively modeled as the deepest boundary nesting, regardless of literal references). Transforms such as Distribution can effect relative clustering of variables within N-nested parens.