BUSINESS STRATEGY TECHNICAL PLANNING COMMENTS
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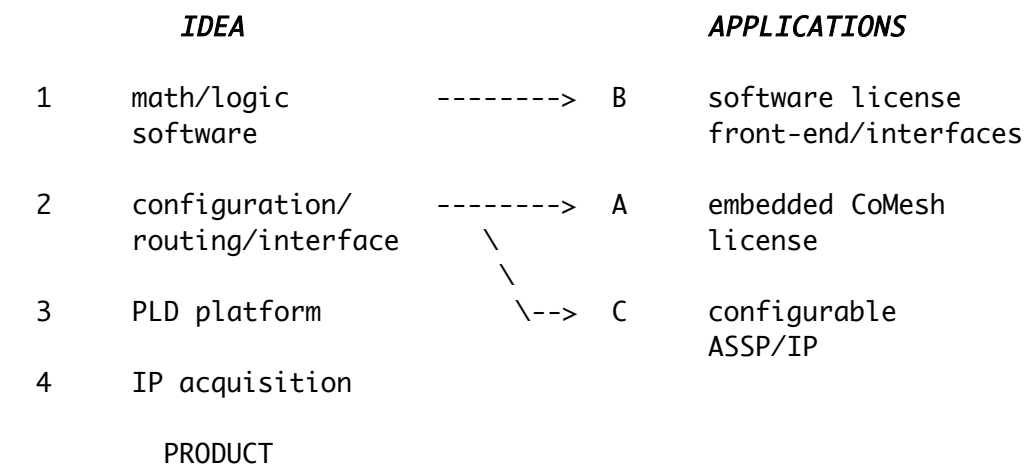
MODEL



PATHS

1-->B	BL software tools
1-->2-->A	CoMesh embedded application
1-->2-->C	CoMesh ASSP/IP application
1-->2-->3-->4	CoMesh co-designed silicon/software product

Paths show dependencies, but do not necessarily imply sequential development.

Math/logic software includes back-end and in-house software development and testing tools.

Path 1-->B enhances in-house development tools to provide front-end products that can be integrated into existing software tools for optimization of logic and routing, primarily for custom and cell-based ASIC design.

Path 1-->2-->A integrates CoMesh silicon capabilities at the block level with in-house software tools to provide a custom package for incorporating CoMesh blocks into ASIC chip environments. In-house software would need to be extended in two ways: 1) add an interface for programming CoMesh blocks in an ASIC design environment, and 2) add additional ASIC design tools to integrate and test CoMesh blocks in the context of an ASIC chip.

Path 1-->2-->C integrates CoMesh silicon capabilities at the block level with in-house software tools to provide a configurable ASSP product. In-house software would need to be extended in two ways: 1) add customization tools for CoMesh blocks, and 2) add additional ASIC design tools to integrate and test CoMesh blocks in the context of an ASSP chip. Additional hardware staff is also needed for ASSP components that are not part of the CoMesh product development.

Path 1-->2-->3-->4 is the CoMesh FPGA product as detailed by the non-augmented BTC business plan. The other three paths are augmentations of this plan to achieve more robust early revenue scenarios.

TECHNICAL RESOURCE ANALYSIS SUMMARY

1. All paths require a full complement of ILOC in-house design, optimization, development and testing tools.

2. Only path **1-->B** does not require a full complement of CoMesh place&route and configuration software tools.

3. All augmentation paths add additional software requirements in order to integrate into chips that include a majority of non-CoMesh components. The extent of additional software depends upon two major factors: 1) the amount of design integration between CoMesh and non-CoMesh components, and 2) the amount of partner support for the integrated product.

3a. Design integration: A black-box ILOC integration approach would permit static design integration using shared files. ILOC would be called sequentially for optimization purposes. Tighter integration into the ASIC design chain would require code customization and substantive partner support. Almost all in-house ILOC development tools would be applicable for all paths. Static design integration provides 90% overlap for these tools, and approximately 50% overlap for interface tools.

3b. Software partner support: The black-box ILOC approach implies development of an independent commercial software capability by BTC, although the customer base may be limited to a few partners. The interface to the BTC software capability could come from an external third-party software vendor who integrates the ILOC core into an existing product.

3c Silicon partner support: CoMesh blocks cannot be considered to be "black-box" due to design and testing integration questions for embedded components. CoMesh blocks are as likely to be customized in an embedded application as they would be in an ASSP application. Silicon partners provide all peripheral silicon components, reducing the development effort of a CoMesh chip by approximately 50%. Almost all CoMesh silicon development infrastructure is applicable to both CoMesh paths.

4. It is expected that partner developed ASSP applications would require deep integration with BTC silicon and software capabilities. ASSP applications should be viewed as specializations of the embedded approach. If BTC elected to market its own ASSP products, separate technical development and support staffing would be required for each separate product.

SELECTED DETAILS OF THE TECHNICAL RESOURCE ANALYSIS

The assumption here is that the CoMesh development path is not decreased from its current minimum. Thus, all augmented paths are additions to existing resource budgets.

Path 1-->B ASIC ILOC Software

Add one additional senior software engineer in month 4 to augment tool designs for this application and to liaison with potential users. Add two junior software engineers in month 4 for ASIC application interface and integration tools.

ILOC internal development tools to be completed in month 7 are not impacted. Interface and documentation requirements for ILOC tools are increased in scope to cover ASIC/ILOC application development after month 7, and are covered by the three additional software staff above. ASIC software prototype deliverable is in month 13.

Path 1-->2-->A Embedded CoMesh

Add one senior hardware engineer in month 4 to augment silicon designs for embedded application and to liaison with potential users. Add one junior hardware engineer in month 4 to specialize in CoMesh embedded customizations. Add one junior software engineer to customize ILOC code, testing, and documentation for embedded applications.

CoMesh design and development is not impacted; peripherals design is independent of the embedded tasks, and block design is slightly generalized. Partner liaison is expected to significantly increase demands on hardware staff and is covered by the additional senior engineer. Embedded deliverables would largely be dependent on partner assistance, liaison, and integration, and should be expected to be ahead of CoMesh product deliverables by not more than about two months. The deliverable prototype embedded architecture would be available in month 15. Earlier delivery is not feasible since the BTC engineering staff would not be sufficiently familiar with the behavior of CoMesh blocks to provide adequate support for partner development.

Path 1-->2-->C Configurable ASSP/IP CoMesh

BTC It is assumed that ASSP applications are an augmentation to the CoMesh strategy, and may be either supported by a partner or developed as product within BTC. The configurable ASSP approach is not substantively different wrt resource needs as is the embedded CoMesh application, except that specialized peripherals for an ASSP product would require separate and additional resources, both for staffing and for silicon fabrication.

Add one senior hardware engineer per reconfigurable ASSP application for specialization of CoMesh to a particular product in month 3 and/or for a particular BTC partner to begin at inception of the ASSP partnership. Add one junior hardware engineer and one junior software engineer per ASSP application. Add hardware staff sufficient to cover specialized peripherals for an ASSP chip.

CoMesh software should be expected to incorporate ASSP application uses independent of actual ASSP commitments, however, the level of additional responsibilities would depend upon the level of integration that a partner may require. On average, the support staff provided by a partner should cover additional BTC loads, with the increase falling primarily on BTC management. In-house ASSP products would require separate management and marketing resources.