WHAT WE HAVE DONE BULLETS

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BTC IP combines two fundamental branches of mathematics
topology and computation
into one uniquely powerful tool
iconic computation
for application to
the design and manufacturing of semiconductors.

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Soft and Hard

BTCIP simplifies computation both

for design of semiconductors (EDA tools)
and
for performance semiconductors (new hardware)

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The EDA Application

With its design products, BTC can control in detail

what a circuit does (its function, its computation)
and
what a circuit looks like (its structure, its topology).

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The Semiconductor Application

With its semiconductor products, BTC can improve

what a circuit does (new functionally, new capability)
and
what a circuit looks like (new design tools).

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What We Offer

Logic synthesis (CDE product):

a minimal functional template with
easy generation for design exploration
easy abstraction for control of scale
easy modification for technology mapping

Physical circuitry (OccA product):

a generic silicon substrate with
complete reconfigurability
full backward compatibility to all existing designs
automated programming (weeks turn to minutes)
high manufacturing yield (homogeneous architecture)

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What We Have for EDA

An elegant and efficient model of circuitry

strongly related to netlists (fully backward compatible)
better multilevel design tools (true Boolean optimization)
easy to use data structure (scales for large designs)
incremental design (fine-grain transformations)
automated circuit generation (parameterized exploration)
better control of timing and routing

A reprieve from several limitations of current EDA tools.

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What We Have for Semiconductors

An elegant and effective model of computation

manufacturable by current practices
competitive in speed and efficiency
low power solutions
reconfigurability solutions
simulation solutions
manufacturability solutions

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Technology

We are enthusiastic about the BTC IP and
we are confident we can manufacture it today.

Here is how we can make money with it
- Market
- Manufacturing
- Merchandising

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The Circuit Design Engine (CDE)

total control over the structure of a given functionality

identifiable sweet points in a design

- very fault-tolerant
- high transistor efficiency (optimal speed and power)
- low energy use
- pipelined data flow
- PLA place and routing
- ASIC manufacturability

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The Occlusion Array (OccA)

total control over the execution of a given functionality

identifiable sweet points in a computing platform

- full backward compatibility
- instant reconfigurability
- automated programming
- high manufacturing yield
- remove timing and wiring complexity from design

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A New Conception of Hardware Architecture

Synthesis:
    The CDE provides automated generation of parameterized functional models

Timing:
    The OccA read-compute cycle standardizes timing across all semiconductor architectures and designs

Wiring Complexity:
    Wires are virtual, simply locations in a memory

RESULTS:
    drastic reduction in design time-to-market
    enormous improvement of hardware performance
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Market Desirability

EDA:
    solves existing limitations in EDA tools
    improves design flow
    greatly improves time-to-market

Semiconductors:
    solves existing limitations in ASIC architectures
    improves manufacturing flow
    greatly improves time-to-market

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Manufacturing Desirability

EDA:
    CDE is currently operational
    6 months to money

Semiconductor:
    OccA is currently operational as a software simulation
    12 months to hardware product prototype
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Merchandizing Desirability

CDE (EDA):
IP approach
license to market leader
no end-user or product distribution responsibilities
efficient non-diluted cash flow early

OccA (semiconductor)
either IP approach or vendor approach
market control of soft-circuitry (OccA data structures) as IP
market control of OccA hardware (exclusive, pioneering patent)
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