BTC PRODUCT STRATEGY

William Bricken
June 2001

"...the increasing use of CAD [Computer Aided Design] means that instead of spending time fighting with soldering irons and test clips, many designers can now spend their time fighting buggy programs running in a buggy software environment."

-- John Wakerly (Cisco and Stanford), Digital Design, 2001

BUSINESS PLAN OUTLINE

BTC has developed a body of new and innovative algorithms for performing computation. These techniques provide new hardware and software architectures with significant commercial advantages. BTC intends to produce a family of product lines, in both hardware and software, which apply our exclusive IP techniques to the computer industry. Initially our market focus will be on a single high performance hardware product.

Foundations

The BTC business plan rests on three foundations:

1. Initial corporate focus on a single innovative product with the greatest market potential.

2. Rigorous and thorough patent protection of the novel IP.

3. Stealth development of diverse product lines based on the novel IP and supported by revenues from the focus product.

We believe that investors have the right to see our best product come to market rapidly, providing opportunity for short-term profitability as well as revenue stability for long-term development of an extensive product line.

The Product

Memory Occlusion Computing (MOC)

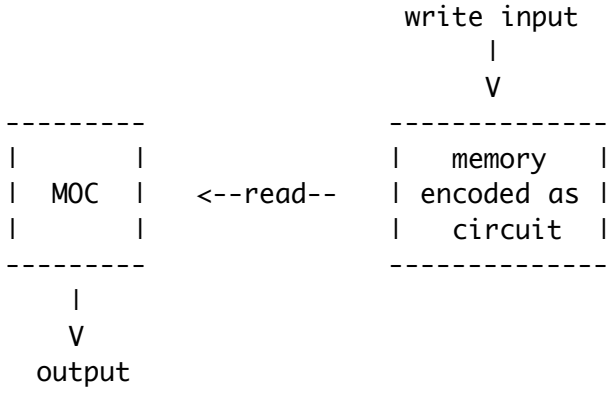
MOC consists of two separate technologies

- a small hardware processor possibly housed on an add-on board, and

- an innovative encoding of hardware functionality as a configuration in standard DRAM or SRAM.

The MOC processor is a small, inexpensive general purpose CPU which processes a software program stored in memory. The program is not a list of compiled machine instructions, rather it is a functional description of a hardware circuit. MOC executes the hardware description at hardware speeds, while the description itself is as reconfigurable as any software program. The MOC processor uses a special read cycle to compute the output of the stored circuit functionality. Thus MOC resembles both a hardware simulator and an reconfigurable hardware device.

The MOC encoding technique converts a circuit description into a binary array in memory. Each wire becomes a 1 in the memory array, each gate and each register becomes a column in memory. MOC encoding removes both wiring and timing design constraints from hardware, converting both into a software data-structure. The encoding technique is backward compatible to any circuit netlist.



INTELLECTUAL PROPERTY

- Architecture of the MOC processor
- Memory encoding techniques

After IP protection, our business strategy includes being opportunistic about the relative merits of licensing vs manufacturing. Several configurations are available, commitment to any would be premature.

- license MOC processor technology and separately license the encoding technology.
- license hardware and sell software encoding
- manufacture and sell hardware, license software encoding.
- bundle hardware and software rights for licensing
- hold all technologies internally for BTC products

Suggested strategy

Seed Round ($600K, 4/01-8/01)

- Comprehensive IP protection
- MOC product definition and prototype
  -- hardware processor
  -- software encoding
- MOC software simulation
- MOC market analysis
- Identify senior management team, hire some on sweat equity
- Identify technical team

First Round ($1400K, 9/01-3/02)

- Build corporate infrastructure
- Open small corporate office
- Hire technical team and round-out management team
- Complete encoding software
- Complete MOC hardware prototype
- Hardware performance comparison demo
- MOC market placement
- Evaluate licensing options
- Keep all technologies stealth

PERFORMANCE ESTIMATES

Size

In a flat architecture using standard memory, N logic gates (and registers) require N^2 bits of memory. A hierarchical architecture would require specialized memory chips with a manufactured cost perhaps double the cost of standard RAM. N gates are estimated to require N^1.5 bits of memory.

The following table compares circuit size to required memory in Mbytes:

number of gates	flat architecture size of memory	hierarchical architecture size of memory
2000	.5 Mb	.1 Mb
5000	3.	.4
10000	12.5	1.
50000	300	11
100000	1.25 Gb	32
500000	30	350
1000000	125	1. Gb

Speed

Processing speed is approximately 4 times memory read speed, around 500 ns. This is two orders of magnitude slower than ASIC gate speeds, and one order of magnitude slower than circuit evaluation speed. Again, a specialized memory architecture could reduce compute time to around 50 ns, which is equivalent to current hardware speeds for non-pipelined circuits.

At 500 ns compute cycles, a MOC could perform 2 million circuit evaluations per second, independent of circuit size, complexity, wiring, and timing.

Cost

A manufactured MOC processor chip should cost a few pennies. If the processor were fabricated on the memory chip, the additional cost would be negligible.

MARKET

MOC outperforms all current FPGA architectures, without requiring hardware layout and fusing. This is a $2B/year market, projected to grow to around $6B by 2005. In competition with FPGAs (Xilinx, Altera, Lucent), MOC provides

- broader functionality
- easier reconfigurability
- automated layout (software memory encoding)
- total backward compatibility
- an order of magnitude less expensive for similar speed
- an order of magnitude faster for similar cost

MOC is an order of magnitude slower than ASICs. In competition with standard ASICs, MOC provides

- reconfigurability
- minimal design time
- easier verification
- cheaper given pre-existing RAM

Adding the MOC onto a memory chip would move manufactures of memory chips directly into the processor market. A strategic alliance with such a company may be extremely powerful.

OTHER PRODUCTS AND MARKETS

Computer Aided Design

The CAD marketplace can be divided into these tool-oriented sections:

- schematic entry
- HDLs
- HDL compilers, simulators, and synthesis tools
- simulators
- test benches
- timing analyzers and verifiers

The essential point for BTC is that BM technology can substantively improve the back-end performance of each of these application areas, however the BM component is about 5% of a marketable CAD software product. Thus we must either license BM software or spend considerable resources rebuilding (or buying) CAD interaction tools and infrastructure.

BM will be quite difficult to integrate into existing CAD backends and algorithms, since the supporting data structures are very different. Most likely, BM would be used as a stand-alone process (perhaps post-process) aiding design. It could be used as a market differentiater for the right CAD company.

Theorem Provers

Losp is essentially a theorem prover. The market for theorem proving technologies is not strong. It includes applications for

- VLSI circuit design and verification
- software construction and verification
- interactive, distributed, and fault-tolerant computing
- knowledge-base and expert systems
- database query optimization and deductive databases

The essential point for BTC is that theorem proving technologies are very difficult to learn and to integrate into standard products. Most theorem provers, including very sophisticated ones supported by the US government, are freeware. Expressing commercial problems in languages usable by theorem provers is extremely difficult.

PITCH

What is the single best initial product for BTC? Candidates:

- license IP
- Losp software enhancement for CAD (Boolean minimization)
- Occlusion Array
- Bit-stream simulator (software)

I believe that any entry into the software market is overtly too weak for our IP position. It also risks undermining our stealth by placing the functional ideas of BM in the hands of others.

Licensing is basically an exit strategy, available anytime. It also fails to capitalize on our potential.

The Occlusion Array pitch is sufficiently strong to support an extensive attempt to attract funding. What we need to modify is

- focus on profitability of OccArray (not on BM or on Bricken)
- limit focus to a single product
- don't mention book, cultural impact, or anything else which suggests dilution of focus
- prepare short product and market description, with timeline and profitability
- use OccArray for a rationale for strong IP protection
- build a prototype, get some accurate performance estimates
- do extensive market analysis
- don't explain or emphasize potential other products

What we need to stick with is:

- MOC is a killer app
- IP protection is broad and paramount, exclusive ownership.
- BM IP provides opportunity for a wide product line, after first product is brought to market
- We control both hardware and software exposure

LESSONS LEARNED

- The competition for investors' money is a candy store.
- Investors want a single focused product.
- New technology requires exceptional improvement (10x).
- Technology products need technical flash, they must catch the imagination.
- For BM, we must buy off on "unusual".
- Investors know that very innovative ideas must struggle against market inertia.
- Our product must address an existing market need, and be capable of attracting existing market share from competitors.