Corporate Overview

Bricken Technologies

December , 2002

Menlo Park, California

FORWARD LOOKING STATEMENTS

This document does not constitute a solicitation or offer to sell securities of the Company.

Some of the matters discussed in this document include forward-looking statements. These forward-looking statements are based on the Company's current expectations and projections about future events. In some cases, you can identify forward-looking statements by terminology such as "will", "expect", "anticipate", "intend", "estimate", and similar expressions (or the negative of such expressions). These statements are based on the Company's current beliefs, expectations and assumptions and are subject to a number of risks and uncertainties. Actual results, levels of activity, performance, achievements and events may vary significantly from those implied by the forward looking-statements.

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Bricken™ Technologies

EXECUTIVE SUMMARY

Bricken Technologies Corporation (“BTC” or “Company”), a Delaware corporation, was established in 2001 to commercialize the Company's novel and proprietary Iconic Logic™ software algorithms and related hardware architectures. These disruptive technologies are the foundation for families of innovative reconfigurable semiconductor products that integrate reprogrammable hardware with highly efficient, implemented software configuration tools. Thus, the Company will provide its customers with a total co-designed hardware/software solution. BTC products are expected to be highly competitive in many segments of the programmable logic device (PLD) market. PLDs are widely used semiconductor components that can be configured for a specific functionality by the end customer. BTC will operate as a fabless semiconductor company. The Company’s hardware products do not require any new manufacturing techniques and rely on standard foundry processes.

The Company's initial product is *CoMesh*™ (*a Computational Mesh*), a reconfigurable block architecture that defines an extensible Field Programmable Block Array (FPBA) product family that is easily customized both for changing market requirements and for specialized market application needs. The CoMesh architecture is a uniform, hierarchical block architecture that is pipelined with five levels of logic. The hardware product is supported by a tightly integrated design tool suite whose capabilities include hardware configuration generated directly from functional specifications, automated dynamic timing closure, multilevel logic optimization, and built-in automated formal verification. The Company’s product line supports all common EDA tool chain and design practices, I/O standards and popular IP cores, and operating systems and platforms. The patent-pending CoMesh FPBA architecture is expected to be highly competitive in the $2.1 billion (2001) programmable logic device market. Within this market, the Company anticipates success in acquiring market share in the market for FPGAs and CPLDs. BTC’s initial customers are expected to be original equipment manufacturers in communications and storage area networks, and perhaps also in the computer, industrial, consumer, and medical segments. In these markets, the principal competitors are Xilinx and Altera.

The Company expects to sell its Bricken-branded hardware products initially directly to OEM and contract manufacturer customers in the United States and through traditional channels abroad. BTC will support its domestic sales efforts and its offshore channel partners with strategic marketing campaigns. BTC will also provide support to its domestic customers and to offshore channel partners, enabling them to support their direct customers.

Principal BTC Value Propositions

CoMesh FPBA integrated hardware/software products provide superior competitive advantages in several areas. These advantages include:

- At least twice the performance for half the price when compared to present FPGA products.
- Speed.
  - Stable 300 MHz (at .18 micron geometry) predictable processing speed.
  - Deterministic timing for multilevel circuits – the benefits of CPLDs in an FPBA.
  - Three times greater user logic gates per mm^2 of silicon than Xilinx FPGAs.
- Fully automated design flow – enter circuit specification and some parameters and the engineer is done.
  - Compatible with major EDA design products.
  - No new skills or design practices required.
  - Backward compatibility with current design practices.
  - Push-button ease-of-use.

- Conventional HDL and schematic capture.
- Guaranteed automated dynamic timing convergence.

- Fast and efficient automated place-and-route
- Formal verification at every step of the design process.

Compared with traditional reconfigurable logic devices, BTC anticipates that its CoMesh FPBA architecture products will have important speed and density advantages as shown in the following table:

	CoMesh FPBAs	**Xilinx Vertex II**
Performance (MHz @.18u)	300	120
Density (user logic gates/mm^2 @ .18u)	1,940	490

BTC's potential products successfully address current industry challenges, including high-speed deterministic timing, integrated formal verification, exceptional ease-of-use, and ultra-fast time to market. In addition, the Company's unique Iconic Logic™ Optimizing Compiler software tool provides unparalleled logic synthesis and place-and-route capabilities.

BTC's Optimizing Compiler vs. Synopsys Logic Reduction

Circuit Description	**Synopsys Internal Pins**	**Iconic Logic Internal Pins**	**Percent Reduction**
Interface to sensors	643	416	35%
Count points on a straight line	840	563	33%
Scramble string / variable cipher	997	652	35%
Compute min and max	1166	722	38%
Elaborate memory contents	1912	960	50%
Viper processor core	10,051	6,012	40%
80386 processor core	19,446	12,335	37%

The table above shows the power of the Company's proprietary software's logic optimization capabilities. For each of seven circuits the table shows the number of input pins to internal logic gates in the EDIF netlist generated from the Synopsys Design Compiler. The table also shows the number of input pins to internal logic gates generated by BTC's proprietary Iconic Logic Optimizing Compiler, and the percent reduction compared with Synopsys.

Stage of Development

The CoMesh FPBA architecture has been completely simulated and tested in software. A first version of the hardware block architecture has been designed at the transistor-level and simulated using SPICE models. A first version of the Iconic Logic Optimizing Compiler is fully implemented and operational. The hardware/software co-design has been verified on hundreds of industry standard benchmark circuits.

Intellectual Property

BTC continues to develop what it expects will be regarded as pioneering intellectual property. BTC has filed several patent applications in the United States and intends to file additional applications in both the United States and in commercially important foreign jurisdictions.

Financing

The Company is seeking a total of $10 million in a Series A preferred equity financing. Of the $10 million, $1 million is seed capital in the form of a Convertible Note financing that includes warrants. BTC intends to use the proceeds of this financing to build engineering, marketing, and sales teams; to acquire hardware and software to develop semiconductor products; to accelerate development of BTC's hardware products and produce customer samples; to develop and implement marketing and sales programs; to acquire first customers and develop strategic relationships; and to protect the company's intellectual property.

To date the Company has raised $500,000. Upon raising the balance of the seed round ($500,000), BTC will engage key engineering personnel and acquire the necessary hardware and software to commence development of the Company's hardware products. Additionally, these funds will be used to obtain and analyze additional market data with respect to finalizing the Company's market entry strategy.

The balance of the Series A preferred round ($9 million) is forecast to take BTC through the production of customer product samples within approximately 15 months and to the acquisition of the Company's first customers.

Summary Financial Information

	Forecast Year				
	1	**2**	**3**	**4**	**5**
Statement of Operations Items (000's Omitted):					
Revenues	$ -	$ 225	$ 15,500	$ 65,000	$ 135,000
Gross Margin	-	(394)	5,425	31,200	87,750
Operating Expenses	3,933	10,822	15,655	25,415	45,225
EBITDA	(3,933)	(11,216)	(10,230)	5,785	42,525
EBIT	(4,097)	(11,798)	(11,536)	1,910	34,417
Net Income (Loss)	$ (3,934)	$ (11,309)	$ (10,838)	$ 3,210	$ 31,188
Balance Sheet Items (000's Omitted):					
Cash and Short-Term Investments	$ 5,124	$ 11,118	$ 17,489	$ 19,309	$ 36,062
Accounts Receivable	-	169	4,030	7,475	13,838
Inventory	-	1,125	9,300	11,375	19,238
Total Assets	6,457	15,320	36,206	54,748	96,192
Shareholders' Equity	$ 5,643	$ 14,184	$ 28,095	$ 31,306	$ 62,494
Other Data:					
Gross Margin	-	-	35%	48%	65%
Headcount	33	69	115	200	320
Revenue per Employee (000's Omitted)	$ -	$ 3	$ 135	$ 325	$ 422
Capital Expenditures (000's Omitted)	1,015	1,680	3,100	14,300	16,875

COMPANY OVERVIEW

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BTC will operate as a fabless semiconductor company. The Company’s hardware products do not require any new manufacturing techniques and rely on standard foundry processes.

The Company's first product is *CoMesh*™ (*a Computational Mesh),* a reconfigurable block architecture that defines an extensible Field Programmable Block Array (FPBA) product family that is easily customized both for changing market requirements and for specialized market application needs. The hardware product is supported by tightly integrated software logic compilation, optimization, and place and route tools.

PRINCIPAL BTC VALUE PROPOSITIONS

Market Challenges Addressed

CoMesh FPBA products provide superior competitive advantages in several areas. These advantages include:

- Lower chip costs and total cost of ownership.
- Exceptional ease-of-use – enter circuit specification and some parameters and the engineer is done.
    - Greatly simplified and automated timing and resource allocation – timing no longer a major issue.
    - Backward compatibility with current design practices.
    - Fast and efficient automated place and route.
    - Formal verification at every step of the design process.
    - Enhanced design flexibility.
- Extensible hardware design.
    - Future products can include embedded microprocessors, substantial memory, and the broadest range of I/Os.
    -

Why CoMesh FPBAs Will Win Market Share

Superior Performance

- Deterministic timing provides stable behavior for faster design turn-around.
- The right balance of logic and interconnect for .13 micron and smaller geometries improves both layout and performance.
- The highly regular block architecture permits greater logic density and higher processing speeds.
- Software and hardware are co-designed using an advanced approach to logic to achieve fast, easy, and efficient synthesis and place and route.

- The CoMesh FPBA architecture is efficient for all types of circuitry.

Faster Time-to-Market

- Stable timing and logic capacity reduce redesign cycles.
- Automated, efficient software for synthesis, layout, and timing reduces design overhead while requiring less expertise.
- Fewer design steps reduces design time.

More Satisfied Customers

- Exceptionally easy-to-use tools reduce design headaches and arduous engineering.
- Less risk improves financial planning and management.
- Lower costs create higher profits for customers.
- Lower total cost of ownership allows customers to produce more competitive products.
- Software/hardware integration makes trouble-solving easier for better customer service.
- Competitive prices for hardware and software.

INITIAL MARKET OPPORTUNITIES

The market for programmable logic devices is large. Semicon Research Group[1] estimates that the global PLD market was $2.1 billion in 2001. Figure 1 shows the vertical PLD market segments as estimated by Cahners In-Stat.

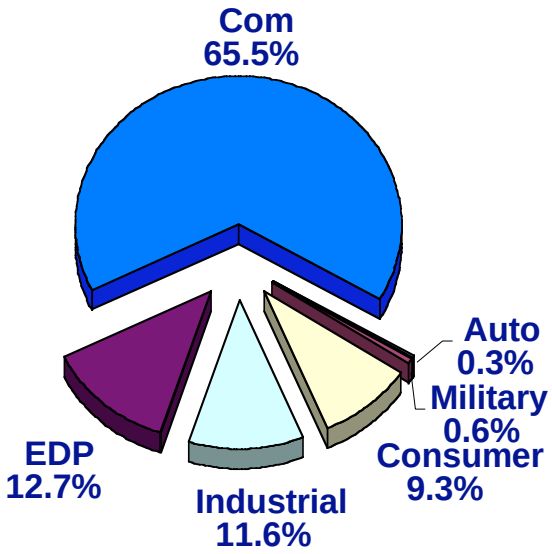

Figure 1: PLD End-Use Markets

[1] Semicon Research Group, “Semiconductor Market Shares”, 2002, pg. 34, (www.semi.org).

The communications application market is by far the largest market segment. Other market segments include computing, industrial, consumer products, military, and automotive applications.[2]

In all markets, the key BTC value propositions are deterministic timing and exceptional ease-of-use, both of which lead to significantly faster time-to-market with reduced development costs. These advantages are expected to be especially attractive in communications markets where product cycles are relatively short and where faster time to market can have a significant positive impact on OEMs.

In recent years the programmable logic market has been divided between Xilinx and Altera, with Lattice, Cypress, Actel and others having little market impact. Figure 2 shows the share of the $2.1 billion PLD market in 2001 by vendor[3].

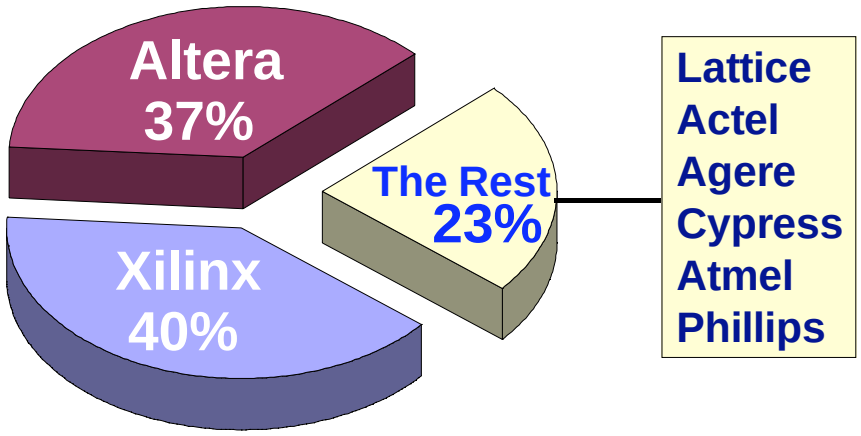

Figure 2: PLD Market Share

A recent Merrill Lynch report[4] identifies Xilinx as the clear leader in the PLD market, with significant momentum compared to Altera. Within the Xilinx product line, the mid-range Virtex-E and Virtex-II lines are believed to provide a significant portion of Xilinx's product revenue and margins.

In a recent survey of 114 designers and other decision-makers in Bay Area OEM companies conducted by a manufacturer's representative firm located in Silicon Valley, 111 indicated a preference for Xilinx and Altera. Market-leading Xilinx had far more committed respondents (59%) than did Altera (18%), while nearly a quarter of respondents (22%) said they were open to both vendors.

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[2] "UPL [User Programmable Logic] Market Forecast: 1999-2004," Cahners In-Stat Group, 2000.

[3] Semicon Research Group, "Semiconductor Market Shares", 2002, pg. 34, (www.semi.org).

[4] Merrill Lynch Flash Note, "Xilinx Inc", May 8, 2002, pg. 1.

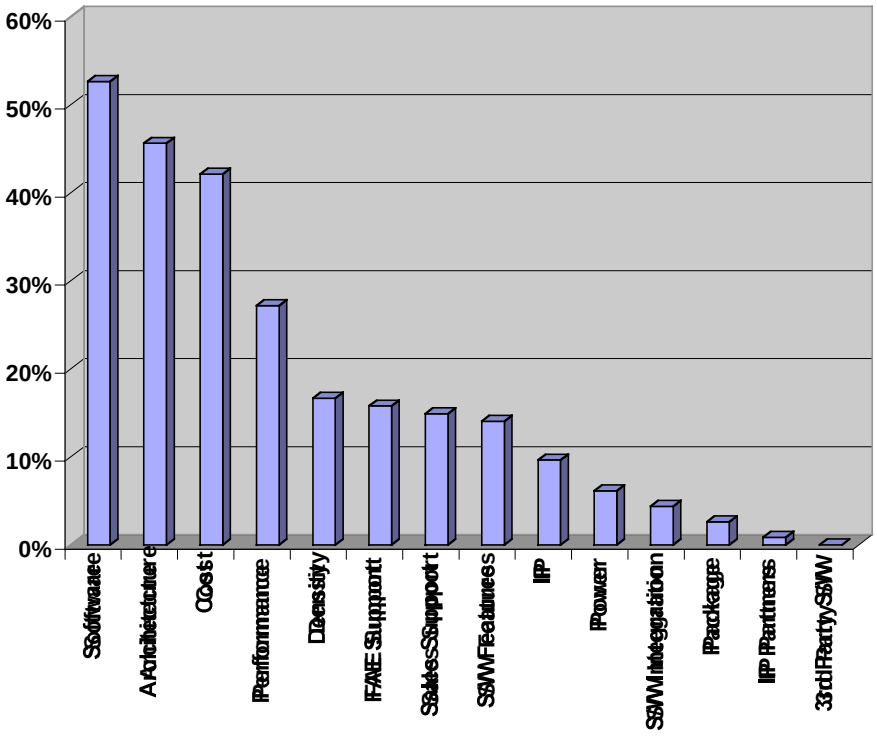

Figure 3: Factors Considered in Switching FPGA Vendors

The user survey also asked what factors might induce decision-makers to change vendors (Figure 3). Slightly more than half of respondents mentioned software as a key factor in their willingness to switch vendors. Architecture, cost and performance were other frequently mentioned important factors. Table 1 summaries the CoMesh FPBA value propositions for each of these factors.

Table 1: Vendor Switching Factors and Key CoMesh Values

Switching Factor	CoMesh Value Propositions
Software	• World-class multilevel synthesis • Co-designed place and route • Automated timing management • Exceptional ease-of-use • Integrated formal verification
Architecture	• Efficient scaleable, modern architecture • Less routing; less routing congestion
Cost	• Significantly reduced total cost of ownership
Performance	• 300 MHz deterministic timing

INTEGRATED HARDWARE/SOFTWARE VALUE PROPOSITION

BTC's primary intellectual property consists of Iconic Logic software algorithms and hardware architectures that create market-disruptive semiconductor product opportunities. Iconic Logic unites logic functionality with geometric layout, providing a circuit design methodology that seamlessly integrates high-performance reconfigurable hardware architectures with exceptionally easy-to-use software configuration tools. The Company has adopted a hardware/software co-design strategy to create its first reconfigurable hardware product, the *CoMesh* Field Programmable Block Array.

The CoMesh platform substantially reduces the engineering effort associated with converting functional specifications to operational hardware. This capability allows product-oriented companies to satisfy their needs for integrated circuitry quickly, efficiently, and inexpensively. Using CoMesh FPBAs requires no new design skills. These benefits provide BTC's customers with a fast, low-risk and inexpensive time-to-market advantage that will enhance their competitive capabilities while lowering their overall engineering costs.

The CoMesh FPBA architecture provides deterministic timing. This means that placement and routing do not effect circuit timing, and timing does not need to be redesigned when the circuit is modified. Deterministic timing promises that a CoMesh chip will meet its timing specifications consistently, without requiring layout and placement design or “by hand” modifications by the end user.

The primary difference between FPGAs and CPLDs is that CPLDs are easier to use, in part because they provide deterministic timing for two-level circuits. They have, however, a fundamental scaling problem, and are not cost-effective for circuits above around 10,000 gates. Larger application circuits require FPGA technology with its accompanying difficult-to-use configuration software. Compared with CPLDs, CoMesh FPBAs offer performance and scalability advantages, while enhancing both design flexibility and ease-of-use.

When compared with FPGAs, CoMesh FPBAs offer important performance, density, design flexibility, verification, and ease-of-use advantages. CoMesh FPBAs also offer the deterministic timing of CPLDs, but for the multilevel circuits that are typically used with traditional FPGAs.

The CoMesh architecture accommodates state-machine and data-flow applications with equal ease, effectively eliminating the functional differences between FPGA and CPLD approaches, while at the same time improving upon the performance and the cost-efficiency of both.

BTC's Iconic Logic configuration tools optimize logic, placement and routing automatically. In contrast, the placement, routing and timing of a given user circuit in a traditional FPGA requires both skill and development resources. Stabilization of timing requires the majority of a design effort. Existing software EDA tools do poorly for timing tasks unless used interactively by a skilled designer who has typically invested a substantial part of their career learning the “tricks of the trade.” As well, unstable timing is a significant difficulty for FPGAs. The timing of a placed and routed design changes whenever that design is modified, requiring that the design be timed again and incurring significant development delay.

Depending on market requirements, the CoMesh FPBA product is intended to be fabricated using a .13 micron geometry, and is designed to scale to smaller geometries as they become available. Manufacturing will rely on standard foundry processes

The CoMesh FPBA architecture has been completely simulated and tested in software. A first version of the hardware block architecture has been designed at the transistor-level and simulated using SPICE models. A first version of the Iconic Logic Optimizing Compiler is fully implemented and operational. The hardware/software co-design has been verified on hundreds of industry standard benchmark circuits.

Comparative Performance

Table 2 compares the performance of CoMesh FPBA with common PLD architectures. The CoMesh metrics were derived from transistor-level SPICE simulation using .18 micron fabrication libraries. For a given level of available logic and for a given level of processing speed, the CoMesh product offers superior value for a reconfigurable architecture.

As indicated in Table 2, the CoMesh architecture improves FPGA performance[5] and density. The CoMesh advantage over FPGAs is stable and predictable performance with higher, more predictable logic densities.[6] The advantage of CoMesh FPBAs over CPLDs is better performance, and scalability to large numbers of logic gates. Not apparent in the chart are the CoMesh architecture advantages of formal verification, efficient automated design, and exceptional ease-of-use.

Table 2: Representative Performance Metrics

	CoMesh FPBAs	**Xilinx Vertex II**
Performance (MHz @.18u)	300	120
Density (user logic gates/mm^2 @ .18u)	1,940	490

USER BENEFITS SUMMARY

Lower Cost Of Ownership

ISSUE: Routing congestion wastes logic resources and degrades timing performance
SOLUTION: **Superior functionality**

- 300 MHz guaranteed for five levels of logic
- automated synthesis/place&route turn-around within hours
- integrated verification to reduce risk in design changes

ISSUE: Traditional FPGA architectures have too little logic, too much routing
SOLUTION: **More user logic resources for the same cost**

- easier and less expensive design integration
- more efficient synthesis and layout for better resource utilization
- sufficient available logic to accommodate almost any user design
- an advantageous ratio of global interconnect to logic

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[5] MHz performance for CoMesh FPBAs are minimal, stable and predictable; MHz performance for FPGAs are average, and can vary greatly as a function of logic and routing.

[6] Logic density for CoMesh architecture is based on assuming 100% utilization averaged over total chip area. For FPGAs, logic gate figures are taken from recent specification sheets, augmented by chip area measurements. When logic is placed in the utilized logic density is assumed to be 6 user gates per 4LUT.

Faster Time-To-Market

ISSUE: Design iterations change timing performance, requiring costly redesign

SOLUTION: **Fewer, faster design iterations without timing changes**

- automated timing closure
- stable timing behavior even as the design changes
- integrated verification prevents design change errors
- preserves reliability of delivery schedules

ISSUE: Changing designs is difficult, time consuming, introduces errors, and is costly

SOLUTION: **Fewer engineering hours to reach design goals**

- incremental design development
- automated test bench validation
- complete, one-step integrated tool chain
- from functional verification to functioning hardware

Superior Ease-Of-Use

ISSUE: Good design takes too much time, too much expertise, and can be very costly

SOLUTION: **Automated circuit generation, synthesis, placement and routing**

- designs generated automatically from functional specification
- designs generated automatically to meet performance specifications
- no additional hand crafted layout work
- no specialized hardware expertise required
- up to 50% reduction in logic for a given functionality

ISSUE: Customers don't want to learn new skills, techniques, or systems

SOLUTION: **Backwards compatibility to all standard tools**

- HDL or netlist in - netlist out
- integrates with conventional tool chain whenever desired
- handles all types of logic with equal efficiency
- locked-down pin assignment does not affect timing or logic capacity
- pin-compatible products

ISSUE: EDA software and FPGA hardware are supported by different companies, lack integration

SOLUTION: **Superb engineering support for an integrated product**

- easier trouble-shooting because of hardware/software co-design
- readily available standard parts, rapid product delivery
- one product from one company for the entire design tool chain

ISSUE: Support of industry standard protocols and capabilities

SOLUTION: **Included on a BTC chip are**

- eight or more clock domains
- internal diagnostics and debugging
- compliant to PCI and other bus protocols
- compliant for almost all I/O protocols and standards
- wide diversity of available IP cores

COMESH BLOCK ARRAY ARCHITECTURE

The CoMesh architecture defines an entirely new class of reconfigurable logic devices that combines the advantages of multilevel ASICs with the efficiencies of simple PLDs. The hardware design is a unique hierarchy of reconfigurable components that incorporates computational cells, larger computational blocks and still-larger block-neighborhoods into an integrated chip architecture.

The CoMesh cell and block architectures have been designed with an emphasis on ease of customization. BTC has designed the CoMesh architecture to be easily modified to meet changing market requirements, and to be easily extended to meet specialized market needs.

For particular application products with moderate volume, both the CoMesh reconfigurable cells and the CoMesh reconfigurable blocks can be customized to meet specific performance objectives, while still retaining the advantages of reprogramability. This approach provides the Company with strategic hardware flexibility that can address rapidly evolving technologies in an ever-changing marketplace.

CoMesh Block Architecture

The basic component of the CoMesh hardware architecture is a *reconfigurable computational cell*. Each cell has the functionality of between 3 to 4 conventional 2-input logic gates.

Cells are arranged into *reconfigurable computational blocks*. One potential block architecture, for example, consists of five rows of sixteen cells per row, and is illustrated in Figure 4 following. Each row of cells communicates with any cell in the row below. Rows of cells within blocks form a *reconfigurable multilevel logic* that is unique among PLD architectures. The final row includes registers that store the computational results of the block, and can potentially return these values to the block input, creating an efficient state machine.

When fully utilized, blocks provide the logical equivalent of about 300 conventional gates. The Iconic Logic place and route algorithms of BTC's Optimizing Compiler can be expected to place and route between 150 to 250 gates in each block. Importantly, blocks are not limited to a single logical function, as many independent functions as can fit into the available cells can be mixed within a single block.

CoMesh blocks optimize computational performance. Regardless of the particular logic or the particular routing within a block, the block delay is a maximum of 2.2 nanoseconds, *for a guaranteed block processing rate of over 450 MHz for up to 300 logic gates*. Blocks are quite small, occupying a silicon area of around .03 mm^2 in a .18 micron geometry. At little cost in either area or speed, CoMesh blocks can include embedded circuitry for specialized functions, such as counters and adders.

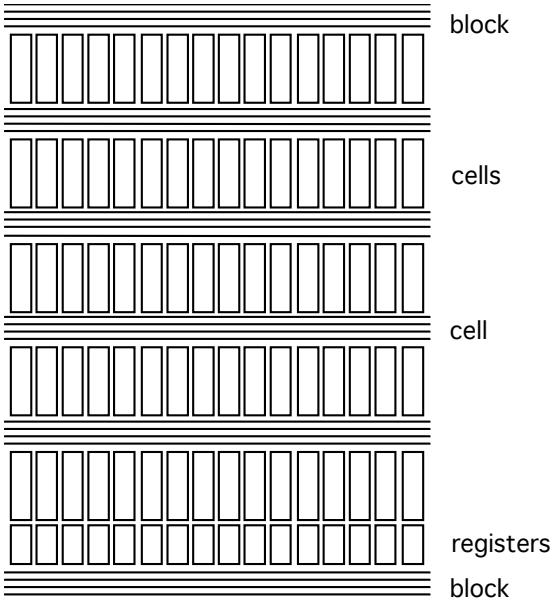

Figure 4: A CoMesh Block Consisting of 80 CoMesh Cells

CoMesh Block-Neighborhood Architecture

CoMesh blocks are arranged into course-grain *block-neighborhoods* of 16 blocks, using the same architectural techniques that arrange cells into blocks. Each block-neighborhood provides the functionality of around 5,000 logic gates, and occupies about 1 mm^2 of silicon in a .18 geometry. The Optimizing Compiler identifies efficient partitions within large logic functions for assignment of logic to blocks within neighborhoods. These partitions minimize processing delay, routing, and routing congestion. The block and the block-neighborhood architectures have been optimized to the capabilities of the Company's proprietary Iconic Logic software synthesis algorithms.

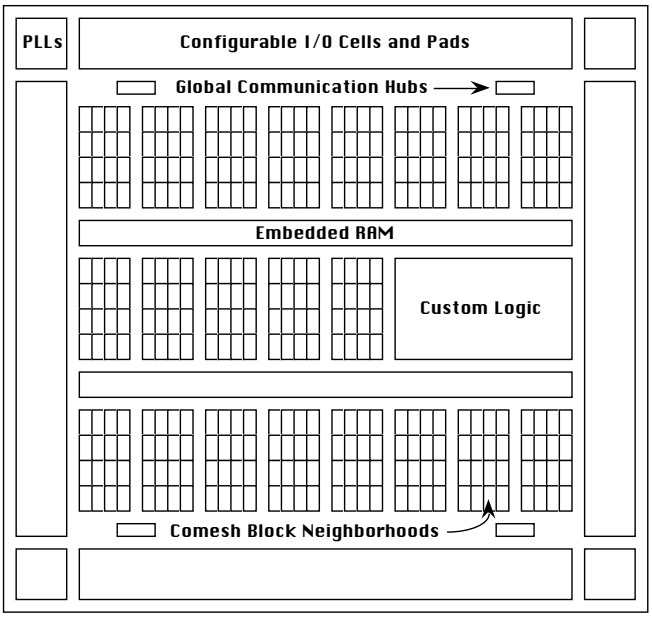

Figure 5: Component Diagram of a 100,000 Gate CoMesh Chip

The fine-grain architecture of both FPGAs and CPLDs requires hundreds of logical units to capture the functionality of 5,000 logic gates. Routing signals between hundreds of these units becomes a nightmare of wasted resources and indeterminate processing delays. The CoMesh software, on the other hand, treats 5,000 gate block-neighborhoods as singular computational units, an approach that resolves problems of both global routing congestion and global routing delay.

A component diagram of a 100,000 gate CoMesh chip is presented in Figure 5 (this diagram is conceptual and is not intended to represent the physical layout of components on a CoMesh chip). The processing core of the chip consists of 21 block-neighborhoods, channels for global routing between block-neighborhoods, and global communication hubs that facilitate rapid global routing. The global routing design assures that any block in any neighborhood can communicate with any other block in less than 1.1 nanoseconds. Adding the 2.2 nanosecond processing delay for a block, the minimal processing speed of the chip is 3.3 nanoseconds, or approximately 300 MHz.

The component diagram in Figure 5 also shows various peripheral support capabilities. These include configurable I/O cells and pads, four global clocks controlled by phase-locked loops (PLLs), resident block RAM, and other specialized embedded functions (Custom Logic). The amount of on-chip RAM is flexible, and will be determined by market requirements. Specialized embedded functions depend upon specific target markets. For example, a DSP-oriented CoMesh chip may include embedded multipliers, while a process control-oriented CoMesh chip may include an embedded microprocessor.

CONFIGURING COMESH HARDWARE

BTC's Iconic Logic Optimizing Compiler software automatically translates a functional circuit specification into the configuration bits for CoMesh hardware. Figure 6 shows the configuration process. Figure 6 also illustrates a consequence of the Company's hardware/software co-design strategy: completely automated software permits end-users to progress from specification to high-performance hardware functionality with exceptional ease. The software optimization and layout tools are intimately connected to the hardware architecture, greatly enhancing the performance of both.

The Iconic Logic Optimizing Compiler uses a unique mathematical technique called *Boundary Logic* to express the functionality of a circuit. This technique is extremely efficient in both logic optimization and in logic placement and routing. The Iconic Logic software integrates both logic functionality and logic layout into a single data structure that provides exceptional flexibility in allocating various logic components to physical computational and routing resources.

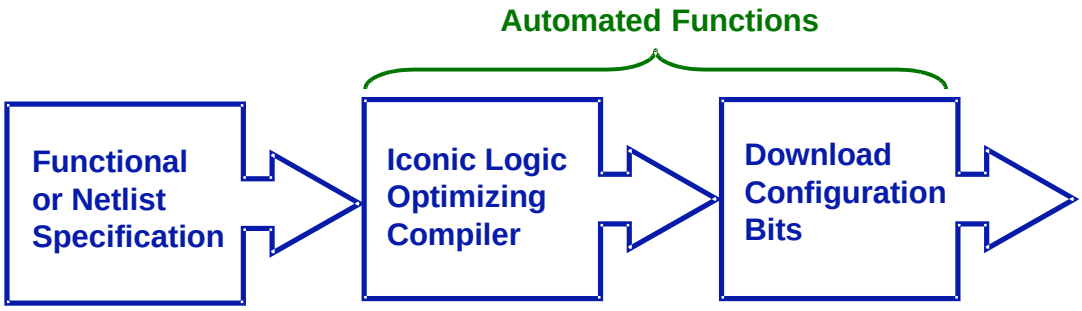

Figure 6: Configuring CoMesh Hardware

The CoMesh hardware architecture was designed specifically to take advantage of the capabilities of Iconic Logic algorithms. The hardware and the software combine to create a seamless unit that bridges the gap between software design and hardware efficiency.

Currently, semiconductor design is split in two, with hardware companies providing physical architectures and software companies attempting to fit functional specifications into these architectures while maintaining the efficiency of the physical components. This split is particularly dysfunctional for PLDs, all of which achieve reprogramability using two-level logic techniques -- look-up tables (LUTs) in the case of traditional FPGAs, and product terms (macrocells) in the case of CPLDs. Hierarchical multilevel circuit designs in software must be artificially partitioned into two-level PLD hardware architectures. CoMesh solves this problem by using a multilevel logic architecture that is tightly integrated with multilevel logic design.

Traditional circuit design software suffers, as well, from an artificial distinction between *technology independent* logic synthesis and *technology dependent* logic layout. This distinction was at one time a convenience, since logical functionality could be addressed by algorithms that did not need to be customized for dozens of different hardware architectures. BTC has applied the techniques of hardware/software co-design to optimize logic for hardware performance, and concurrently to optimize hardware for logic synthesis. Nevertheless, an imperative BTC design constraint was to maintain compatibility with existing design practices and fabrication techniques.

The Iconic Logic Optimizing Compiler

The Iconic Logic Optimizing Compiler takes as input an industry-standard functional or netlist description of circuit specifications. Compilation is rapid and automated, resulting in a file containing the configuration bits used to program the CoMesh hardware. Inside the Optimizing Compiler, the functionality of a circuit is converted into a proprietary Iconic Logic representation, and reduced to an optimal form for placement and routing in the CoMesh hardware.

Table 3 shows the power of the Iconic Logic Optimizing Compiler's logic optimization capabilities. For each of seven circuits,[7] the table shows the number of input pins to internal logic gates in the EDIF netlist generated from the Synopsys Design Compiler. The table also shows the number of input pins to internal logic gates generated by BTC's proprietary Iconic Logic Optimizing Compiler, and the percent reduction compared with Synopsys.

Table 3: Optimizing Compiler vs. Synopsys Logic Reduction

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Compute min and max	1,166	722	38%
Elaborate memory contents	1,912	960	50%
Viper processor core	10,051	6,012	40%
80386 processor core	19,446	12,335	37%

Time-to-market is often of primary importance since it frequently determines the shelf life of most networking and computing hardware. This is where the Company's Iconic Logic Optimizing Compiler excels:

[7] These circuits and the Synopsys netlists are from the International Test Conference (ITC'99) benchmark panel for RT-level automatic test sequence generation.

- The Iconic Logic configuration software incorporates formal verification in every step, assuring that a design does not stray from the functionality defined in the circuit that is the input to the Optimizing Compiler.
- The Iconic Logic software is fully automated, allowing a designer to go from specification of circuit functionality to optimized functioning hardware within the same day.
- Due to the homogeneous CoMesh architecture, a configuration produced by the Iconic Logic software will have predictable and stable timing and logic density, even as a user circuit design is changing rapidly during iterative refinement.

To use CoMesh FPBA hardware, a designer need only specify the desired logic functionality using any standard functional specification language such as Verilog, netlists, logic equations, or finite state machine descriptions. Once design functionality is specified and entered into the Optimizing Compiler, all other user design steps, including timing, are unnecessary. The Optimizer automatically provides functional synthesis and CoMesh hardware configuration bits.

The algorithmic power of the Optimizer was used to guide CoMesh hardware architecture design decisions; the deterministic behavior of the architecture guides the software optimization process. The hardware/software co-design strategy achieves both hardware and software efficiency while greatly reducing the complexity of the engineering design process. The result is a circuit design tool with exceptional ease-of-use combined with hardware of exceptional performance and flexibility.

Iconic Logic

Iconic Logic is a mathematical innovation that has no prior history of implementation in software or in hardware. The idea itself, however, is over 100 years old, and can be traced back to the works of the American logician Charles S. Peirce and the German mathematician Gottlob Frege, who is credited with the invention of formal mathematics. Both Peirce and Frege developed formal logical systems that incorporated spatial, geometric aspects. These powerful techniques were lost when computers that processed strings of binary symbols were invented, since binary strings do not convey geometrical information.

Iconic Logic unites logic, geometry and algebra in unique ways. The essential innovation is that Iconic Logic is *simpler than* conventional logical approaches. This leads to computational algorithms that are less complex and chip architectures that use simpler computational processes. The simplicity is achieved by expressing the concepts of computational logic in two-dimensional spatial, geometric terms rather than in conventional one-dimensional symbolic strings.

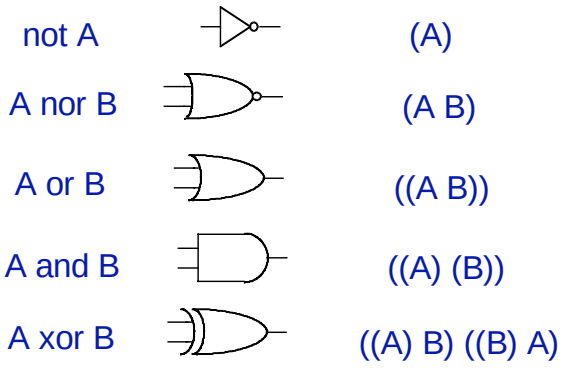

Figure 7: Converting Logic Gates To Iconic Logic

Figure 7 provides a formal map between the conventional logical connectives, conventional logic gates, and the spatial representations of Iconic Logic. The right-most column shows Iconic Logic forms that are equivalent to the

conventional logical forms on the left. Iconic Logic can be expressed solely in terms of parentheses and input tokens.

The simplicity of Iconic Logic is visually obvious in Figure 7. Although conventional logic requires many different connectives, and conventional logical gates come in many different forms, Iconic Logic consists of only one type of mathematical object, a spatial container. To express all of the computational concepts of logic, it is sufficient to construct different configurations and nestings of simple parenthesis delimiters. The Iconic Logic parenthesis data structures require only sorting and pattern-matching algorithms. These algorithms are very well known, and importantly, do not involve computationally expensive searching processes.

BUSINESS MODEL

BTC will operate as a fabless semiconductor company. The Company expects to sell its Bricken-branded hardware products directly to OEM and contract manufacturer customers in the United States and through traditional channels abroad Channels include manufacturer's representatives and distributors of electronic components. BTC will support its domestic sales efforts and its offshore channel partners with strategic marketing campaigns. BTC will also provide support to its domestic OEM and contract manufacturing customers and to offshore channel partners, enabling them to provide the necessary front-line support to their direct customers. To encourage adoption of the Company’s hardware products, BTC intends to license its Optimizing Compiler for use with its hardware products without cost or for a nominal fee that is intended to recover support and distribution costs. Software, documentation, and support will be offered over the Internet.

In addition to product revenue, BTC may also license its Intellectual Properties for specific market applications where market size or market structure indicate that licensing is the preferred strategy.

BUSINESS AND OPERATING STRATEGIES

Growth Strategies

- Develop proprietary reconfigurable logic device total solutions that exploit first mover advantages for next-generation PLDs, including ease-of-use, performance, and density, in key vertical markets such as communications and computing.
- Extend, improve, and enhance these reconfigurable logic device total solutions in response to market opportunity and industry/customer need.
- Establish and maintain strategic relationships, including with fabrication, key customers, and channel partners.
- Develop domestic marketing programs focused on decision-makers in OEMs and contract manufacturers.
- Develop offshore marketing programs focused on key vertical markets and channel partners to establish product branding.
- Penetrate key vertical markets through channel partners and other strategic partners.

Operating Strategies

- Develop reconfigurable logic device total solutions targeted on meeting changing customer and vertical market requirements.
- Maintain leading-edge technology and pace product development to customer demand.
- Attract technical, sales, and marketing staff with substantial industry experience and knowledge.
- Provide training and support to BTC's staff and channel partners so they can provide frontline support to customers.
- Create intellectual property and protect it in the United States and in commercially important foreign jurisdictions.

INTELLECTUAL PROPERTY CREATION AND PROTECTION

The Company presently owns and is continuing to develop what it expects will be regarded as pioneering intellectual property. BTC has filed several patent applications in the United States and intends to file additional applications in both the United States and in commercially important foreign jurisdictions. The Company also intends to file trademark applications in the United States and in other commercially significant jurisdictions. Where appropriate, the Company will apply for copyright registration for selected materials.

LEGAL ADVISORS

FINANCING, USE OF PROCEEDS, AND STATUS

The Company is seeking a total of $10 million in a milestone-based Series A preferred equity financing. Of the $10 million, $1 million is seed capital in the form of a Convertible Note financing that includes warrants.

BTC intends to use the proceeds of this financing to:

- Build engineering, marketing, and sales teams,
- Acquire hardware and software to develop semiconductor products,
- Accelerate development of BTC's hardware products and produce customer samples,
- Develop and implement marketing and sales programs,
- Acquire first customers and develop strategic relationships,
- Protect the Company’s intellectual property, and
- Build Company infrastructure including support staff.

To date the Company has raised $500,000. Upon raising the balance of the seed round (an additional $500,000), BTC will engage key engineering personnel and acquire the necessary hardware and software to commence development of the Company’s hardware products. These funds will also be used to obtain and analyze additional market data with respect to finalizing the Company’s market entry strategy. The balance of the Series A preferred round ($9 million) is forecast to take BTC through the production of customer product samples within approximately 16 months and to the acquisition of the Company’s first customers.

The Company’s forecasted financial statements are presented in Exhibit A.

EXECUTIVE MANAGEMENT

William Bricken, Ph.D. — Vice Chairman, Chief Scientist, Director and Founder

Dr. Bricken has spent over 20 years developing the tools and techniques of iconic mathematics. He has published widely in the fields of artificial intelligence, virtual reality, and education. Dr. Bricken was an Assistant Professor of Computer Science and Software Engineering at Seattle University, Seattle, Washington, from 1996 to 2001; Research Associate Professor of Education at the University of Washington from 1992 to 1995; the Principal Scientist of the Human Interface Technology Lab at the University of Washington, specializing in virtual reality design, software, and hardware technologies, from 1990 to 1994; Lecturer in Education at the University of Hawaii at Hilo from 1976 to 1979; Assistant Professor of Social Psychology and Education at the State College of Victoria, Rusden, Melbourne, Australia, from 1973 to 1975; and Principal and Founder of Coonara Primary School, Melbourne, Australia, from 1972 to 1975.

In industry, Dr. Bricken was a consultant to Interval Research Corporation, Palo Alto, California, from 1993 to 2000; CTO of Virtual Express, a virtual reality start-up, in 1994; the first Distinguished Fellow, and Director of the Research Lab at the computer-aided design industry leader Autodesk, in Sausalito, California during 1988 and 1989; Principal Research Scientist at Advanced Decision Systems, which contracted to the US Department of Defense for artificial intelligence research, from 1984 to 1988; and a Wizard at Atari Research Lab, Sunnyvale, California, exploring advanced concepts for gaming, during 1983 and 1984. University of California at Los Angeles, B.A., Social Psychology, 1967; Monash Teachers College, Melbourne, Australia, Diploma of Education, 1972; Stanford University, Stanford, California, M.S., Statistics, 1984; Stanford University, Ph.D., Mathematical Methods of Research, School of Education, 1987.