Iconic Tools Advance the State of the Art for Circuit Optimization:

Breakthrough Performance in Path Delay, Area Tradeoffs

Background

Hardware design tasks are changing rapidly. The EDA tools and techniques that worked well for thousands of transistors do not scale to millions of transistors. Deep sub-micron technology is providing ample computational area, but requires careful wiring optimization. The decreased development time offered by reconfigurable devices is paid for with significantly lower design efficiency and performance. Multi-protocol, multi-mode, multi-function devices are obsoleting ASIC solutions in many markets.

This rapid evolution in the nature of design is taking place in a context for which *time-to-market* and *manufacturing costs* are paramount. There is literally no time left for careful design and no money left for tailored hardware. Designers must achieve both increased performance and faster turn-around while producing inexpensive just-in-time chips. And due to the complexity of designs, designers are completely dependent upon their automated software design tools. Where will the next qualitative jump in EDA tool performance come from?

Iconic Logic™

Common wisdom suggests that the semiconductor industry understands logic, the foundational mathematics underlying all design and indeed all computation. Although the logical networks we work with are known to create complex synthesis problems, in today's sophisticated design environment no one expects that a fundamental change of perspective in the way we use logic itself can significantly improve the circuit design process. Until now!

BTC's circuit design tools implement an entirely new approach to logic, called **Iconic Logic**. Iconic techniques are provably more efficient than conventional techniques, leading to improved scalability of algorithms *in all cases*. This logic is *much simpler,* yet *more powerful* than what is currently used today, providing fast, automated designs that are error-free, verified, and testable.

Iconic Logic Optimizing Compiler (ILOC™)

Design optimization and design flexibility come freely through the simplicity of the new Iconic Logic computational methods implemented in BTC's Iconic Logic Optimizing Compiler (ILOC). ILOC uses a formal *design algebra*, based on a simple non-Boolean mathematics, to produce reduced circuits that meet specified delay and area criteria, automatically. By optimizing both logic and wiring at the same time, ILOC efficiently produces *fully testable* fault-tolerant circuit designs without redundant components, false paths, and reconvergent paths. ILOC employs *formal verification* of every design change, leading to fewer design errors and fewer design cycles. ILOC integrates synthesis with technology mapping, providing efficient designs for selected target architectures including ASICs and FPGAs.

Breakthrough Technology

Iconic Logic provides a basis for the next breakthrough circuit design technology. The ILOC implementation of Iconic Logic is completely backward compatible with existing design techniques and existing circuit specifications. Learning new skills and mastering new tools is not necessary. Designers can go from functional specification to verified netlist at the push of a button, while generating designs with superior performance.

Consider, for example, the delay performance of a particular design. The time that it takes for a signal to propagate along the longest path in the design determines its *critical delay*. Delay reduction requires transforming the structure of the transistor network into one that has a shorter critical delay. Delay is influenced by the number and types of gates along the critical path, by the length and fanout of wires, by the particular combination of input pins and outputs pins along the critical path, and by numerous other factors related to the physical structure of a network and its resistance to current flow. All of these factors must be considered when improving delay performance.

Breakthrough Performance

ILOC reduces the best delay performance of an industry leading competitor by an average of 12% over a diversity of designs, at a cost of an additional 17% in area. ILOC also reduces the competition's best area performance by an average of 18% when delay is not an important design consideration. Many designs require a balance between delay and area; for these, ILOC provides an average delay reduction of 8% at an area cost of just 7%. Unlike other commercial systems, ILOC permits a designer to steer the engine performance through a diversity of delay and area trade-off points, selecting the performance that is most desirable for a particular design.

These demonstrated gains are the result of the way that Iconic Logic provides order to network transformation rules, and the way that ILOC implements these rules. In contrast, current state-of-the-art tools and techniques for network delay optimization consist of a haphazard collect of unrelated ideas and algorithms.