LABELLING THE CELL STRUCTURES

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NOTE: no separate block ids as yet

CONVENTIONS:

```
            parameter i labels tier          (1..5)
            parameter j labels cell          (01..32)
            parameter k labels cell outputs  (1..2)
            lambda    # locates input wires  (01..16)
            inverted signals marked with "-"
```

input wires: wi_# with # = 01..16

external input wires: w1_# with # = 01..16

cell outputs: ci_j_k with k = 1..2

cells: ci_j with j = 01..32

tiers: ci_j with i = 1..5

block outputs: c5_j_k
= block register inputs

bypass/inv inputs: wi_#

CONSTRAINTS:

```
            4:1MUX {wi_01, wi_05, wi_09, wi_13}
            4:1MUX {wi_02, wi_06, wi_10, wi_14}
            4:1MUX {wi_03, wi_07, wi_11, wi_15}
```

3NAND inputs wi_# with -wi_# if inv is selected

NOTE: no separate labels identifying which of the three inputs

3NAND output: ni_j

3NAND-inv input: ni_j

3NAND-inv output: ci_j_1 with ci_j_1 = -ni_j

forward inv input: wi_#

CONSTRAINT: one of {wi_01, wi_05, wi_09, wi_13}

forward inv output: -wi_#

2NAND inputs: ni_j and ni_j+1

NOTE: each tier has j-1 2NAND gates

2NAND output: ?

2NAND-bypass-inv input: (MUX 2NAND-output forward-inv-output)

2NAND-bypass-inv output: ci_j_2
= -(MUX 2NAND-output forward-inv-output)

input binding pairing of wire name with input name
<wi_# input-name-ijk>,

CONSTRAINT: <w1_# external-input-name> tier = 1 when external input

NOTE: wires for internal tiers will be *explicitly* bound to cell output names (eg: <w3_7 c2_14_2>) pending a regular architecture for connecting cell outputs to next tier input wires.

CONSTRAINT: <wi1_j1 ci2_j2_k>
with i2 = i1 + 1
except for feedup, in which case i2 = i1
and j1 as any j2 so long as only one j2 per j1
(ie any cell output connects to any wire, only one per wire)
with exception that some specific wire will be designated as the feedup wire.

block register inputs: c5_j_k

block register outputs: w1_#

NOTE: assume any register can be feed back into any external input wire. Will this be standardized? For now assume registers feed back only into same block, or to external.